iND83080 Datasheet
Rev 1.0

1 Document Revision History

Rev #	Date	Action
0.1	2021/1	Initial release
0.9	2022/3	Add register map
0.92	2022/6	Update EC table
1.0	2022/12	Update content, update EC table

2 Table of Contents

3 System Overview

3.1 Introduction

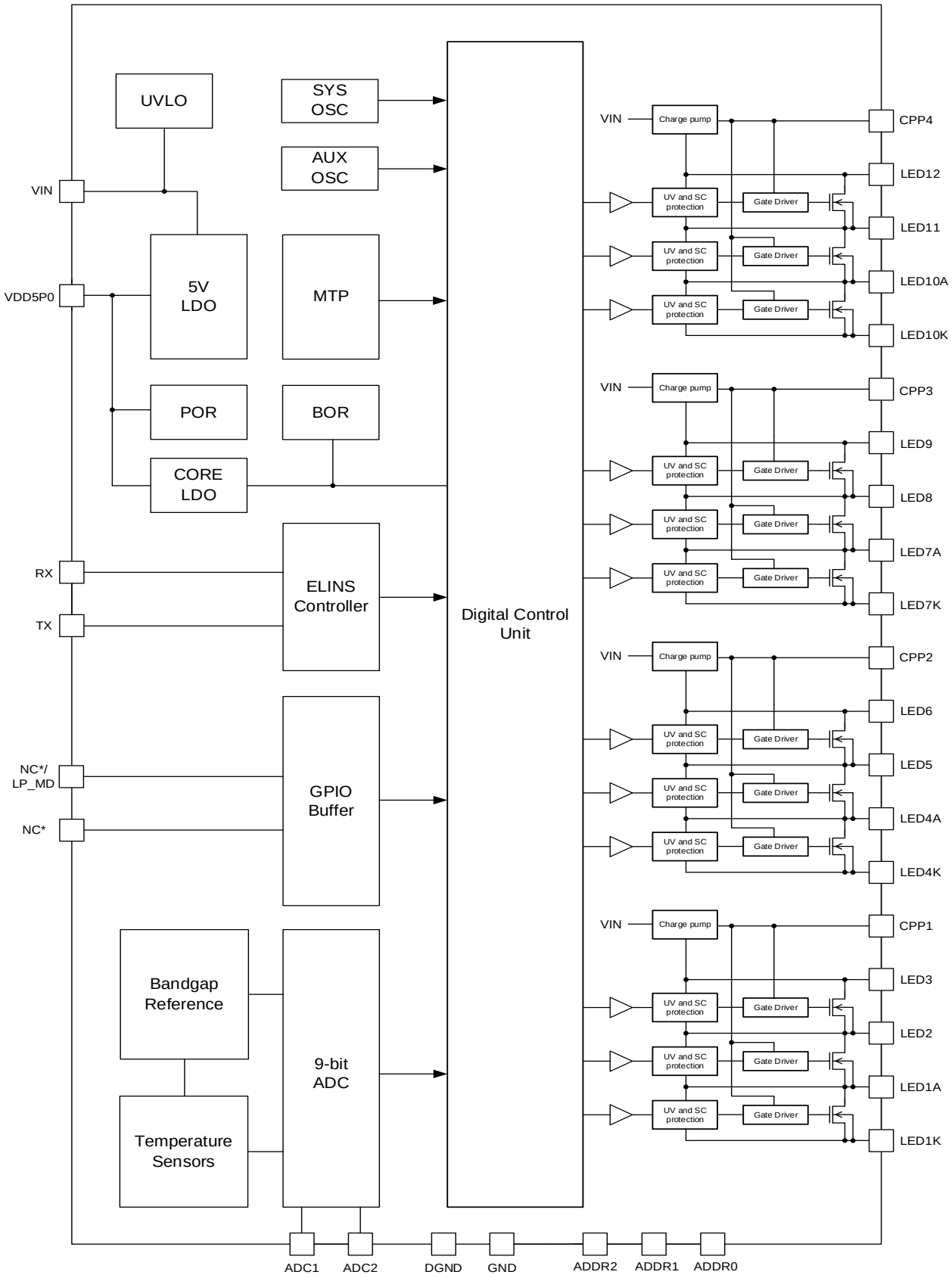
The iND83080 is a high-performance automotive Matrix LED lighting controller, which integrated 4 sub-blocks of 3 series-connected switch MOSFETs. Each switch in the device can be controlled by 12-bit PWM internal signal with configurable slew rate and phase shift. The individual sub-switch block can be configured in parallel to different current sources or in series to one common current source flexibly. The device provides complete LED matrix manage features including switch slew rate control, LED open/short detection and protection, etc. The integrated EMC enhanced charge pump module supplies the gate drive power for each LED bypass switches, the low $R_{DS(on)}$ of the bypass switch minimizes conduction loss and power dissipation. The diagnostic system monitors the status of charge pumps, and there will be an error flag if the output voltage of charge pump is not enough to drive the gate of switch MOSFET.
Multiple iND83080 devices can communicate with master under the same ELINS bus to work together for dynamic scenario. The private protocol ELINS based on UART allows up to 32 devices on an ELINS bus. All the internal clocks are synchronized with the internal oscillator and the calibration is done via the ELINS sync message. This process allows for a very accurate clock (accuracy<0.25%) for communication.
MTP (non-volatile Multi-Time Programmable memory) up to 2Kbit is integrated to store system configuration data and customer data, such as Limp-home Mode settings, Smart Mode PWM curves and Standalone Mode settings. The Limp-home Mode settings are independently configurable for each channel.
The iND83080 also supports Standalone Mode which minimize the design of the host controller with only three digital input signals.
An on-chip ADC with two external single-ended input channels can be used for system temperature compensation and measuring a binning value which allows for LED binning and coding. The ADC can also monitor internal temperature, which is available to be read by the microcontroller via the ELINS interface.

3.2 Main features

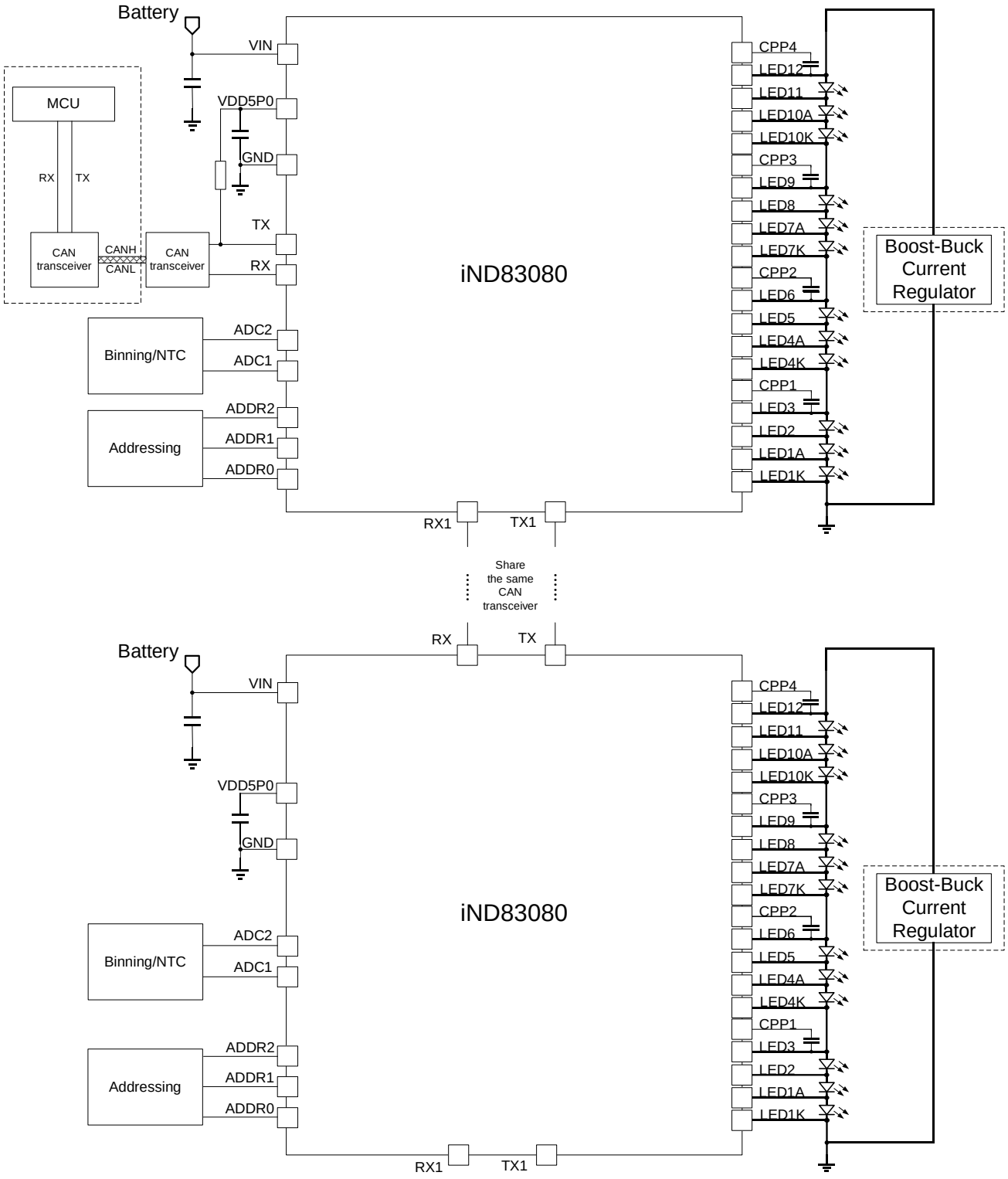
- Full automotive qualification AEC-Q100 Grade1
- 12 channels, grouped to 4 configurable blocks, 3 switches per block
- 170mΩ $R_{DS(on)}$ for each switch
- Support both battery direct supply and external 5V LDO supply
- 12-bit PWM signal with independent channel PWM width control, support both Direct Mode and Smart Mode PWM control
- Private protocol ELINS based on UART up to 1Mbps with CRC, optional external CAN transceiver to improve robustness and EMC
- Support up to 32 matrix IC in one bus, sync by protocol
- High accuracy oscillator integrated with EMC improvement
- Internal MTP up to 2Kbit for system parameters configuration, such as Limp-home Mode configuration
- Internal watchdog and programmable Limp-home Mode in case of communication failure

- Internal over-temperature detection and protection
- On-chip temperature monitor for IC temperature monitoring
- 2 external ADC input channels for monitoring Bin, NTC, etc.
- Slew rate and phase shift control to avoid current spike
- Single LED open/short detection and protection
- Internal charge pump fault detection

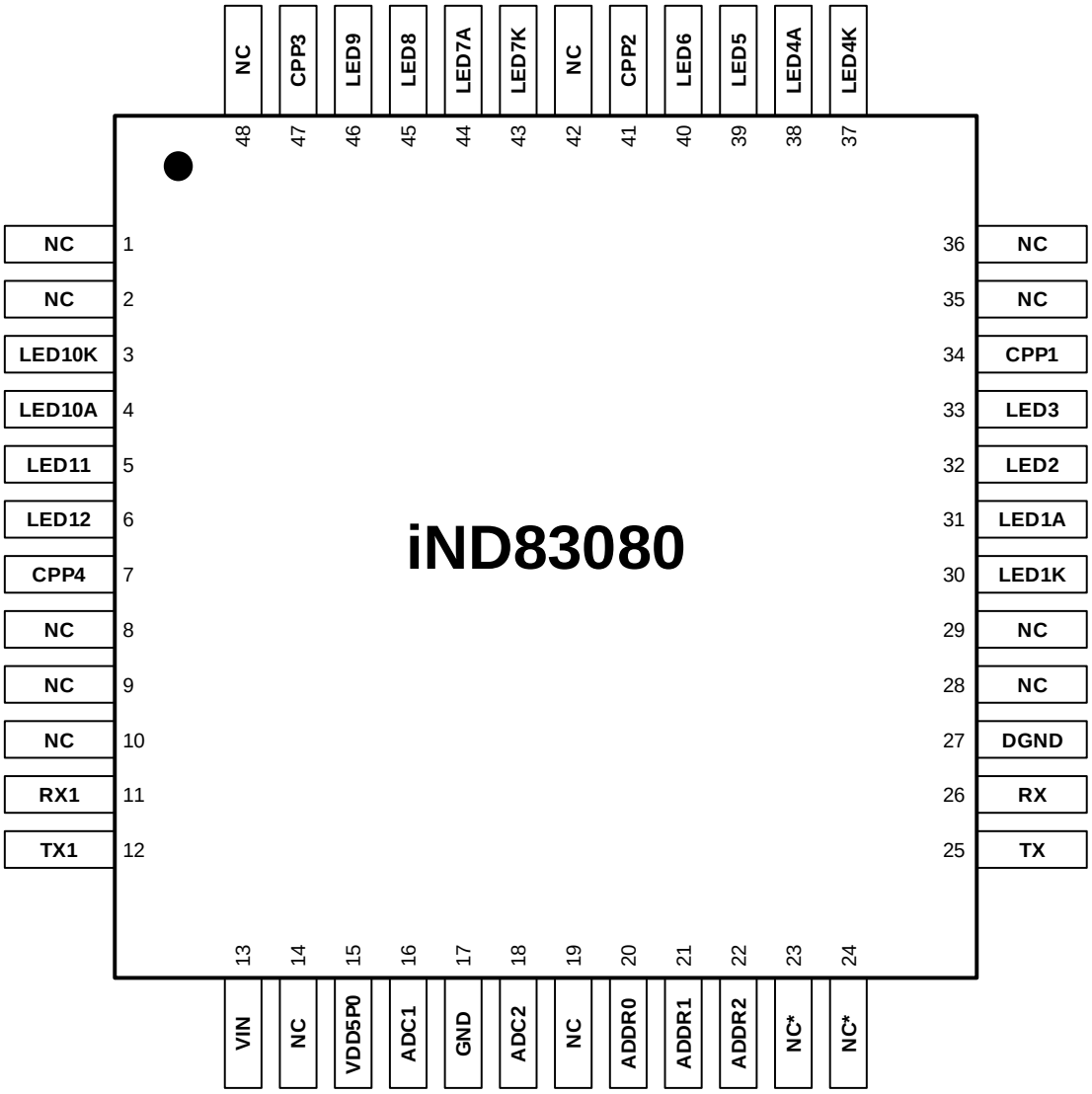
3.3 Functional Block Diagram



3.4 Typical Application



3.5 Pin Configuration and Function



PIN		Type	Description
Name	No.		
ADC1	16	I	ADC PAD_ADC1 channel input
ADC2	18	I	ADC PAD_ADC2 channel input
ADDR0	20	I	Least significant 3 bits of Device ID. Tie to resistors divider from VDD5P0 to get 3 LSB of Device ID. The internal ADC samples the voltage of ADDR0 as the Device ID
ADDR1/S_MODE1	21	I	MSB1 of Device ID. Tie to VDD5P0, or to the ground ('0'). Used as Waterfall Mode trigger pin in Standalone Mode, GPIO1 in MTP settings
ADDR2/S_MODE2	22	I	MSB2 of Device ID. Tie to VDD5P0, or to the ground ('0'). Used as Flashlight Mode trigger pin in Standalone Mode, GPIO2 in MTP settings
NC*/LP_MD	23	I/O	Used as Limp-home Mode trigger pin in Standalone Mode, GPIO3 in MTP settings
NC*	24	I/O	No connection, GPIO6 in MTP settings
CPP1	34	O	Charge pump output. Bypass with a ceramic capacitor with a minimum value of 0.1μF to LED3 pin
CPP2	41	O	Charge pump output. Bypass with a ceramic capacitor with a minimum value of 0.1μF to LED6 pin
CPP3	47	O	Charge pump output. Bypass with a ceramic capacitor with a minimum value of 0.1μF to LED9 pin
CPP4	7	O	Charge pump output. Bypass with a ceramic capacitor with a minimum value of 0.1μF to LED12 pin
GND	17	G	Device system ground. All GND pins MUST be connected for proper operation
DGND	27	G	Digital and communication ground. Tie it together with GND and EPAD

NC	1, 2, 8, 9, 10, 14, 19, 28, 29, 35, 36, 42, 48	NA	No connection
LED1K	30	I/O	Connect to cathode of LED1
LED1A	31	I/O	Connect to anode of LED1 and cathode of LED2
LED2	32	I/O	Connect to anode of LED2 and cathode of LED3
LED3	33	I/O	Connect to anode of LED3
LED4K	37	I/O	Connect to cathode of LED4
LED4A	38	I/O	Connect to anode of LED4 and cathode of LED5
LED5	39	I/O	Connect to anode of LED5 and cathode of LED6
LED6	40	I/O	Connect to anode of LED6
LED7K	43	I/O	Connect to cathode of LED7
LED7A	44	I/O	Connect to anode of LED7 and cathode of LED8
LED8	45	I/O	Connect to anode of LED8 and cathode of LED9
LED9	46	I/O	Connect to anode of LED9
LED10K	3	I/O	Connect to cathode of LED10
LED10A	4	I/O	Connect to anode of LED10 and cathode of LED11
LED11	5	I/O	Connect to anode of LED11 and cathode of LED12
LED12	6	I/O	Connect to anode of LED12
RX	11,26	I/O	Received data pins. Connect one RX pin of the first device to microcontroller unit TX output and use the second pin to connect to a RX pin of the second device. All other devices use both pins to route the RX line through each device. Two pins are connected internally, GP4 in MTP settings
TX	12,25	I/O	Transmitted data pins. Connect one TX pin of the first device to microcontroller unit RX input and use the second pin to connect to a TX pin of the second device. All other devices use both pins to route the TX line through each device. Two pins are connected, GP5 in MTP settings
VDD5P0	15	I/O	Internal 5 V LDO output or external 5V supply input. This pin requires a ceramic output capacitor with a value of 2.2μF or greater
VIN	13	I	Input voltage, connected to battery. Bypass with a ceramic capacitor with a minimum value of 1μF to GND
EPAD	DAP	G	Connect to System Ground

Note:

(1) Pin 23 and Pin 24 are also used for internal test and debugging.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Voltages Referenced to ground.

Names	Conditions	Min.	Typ.	Max.	Unit
VIN		-0.3		60	V
LEDn to LEDn-1	LED1A to LED1K LED2 to LED1A LED3 to LED2 LED4A to LED4K LED5 to LED4A LED6 to LED5 LED7A to LED7K LED8 to LED7A LED9 to LED8 LED10A to LED10k LED11 to LED10A LED12 to LED11	-0.3		22	V
VLEDn to ground		-0.3		62	V
CPP1~CPP4 to ground		-0.3		70	V
Max RMS value per switch		0		1.5(1)	A
ADDR0, ADDR1, ADDR2, TX, RX, NC*(2), ADC1, ADC2, VDD5P0		-0.3		5.5	V
Junction Temperature, T_j	Internal junction temperature	-40		150	℃
ESD(3)					
HBM		-4		+4	kV
CDM		-750		+750	V
Latch-up		-200		+200	mA

Note:

(1) Based on the worst case calculation: max constant current, all 12 switches are on, 125℃ ambient temperature, 7K/W package thermal resistance

(2) NC* is the Pin 23 and Pin 24

(3) This device series incorporates ESD protection and is tested by the following methods:

ESD Human Body Model tested by ANSI/ESDA/JEDEC JS-001-2017

ESD Charged Device Model tested by ANSI/ESDA/JEDEC JS-002-2018

Latch-up tested by AEC-Q100-004-REV-D 2012

4.2 Thermal Information

Parameter	Conditions	Min.	Typ.	Max.	Unit
Operating Temperature, T_a	AEC-Q100 Grade 1	-40	25	125	℃
Storage Temperature		-55		175	℃
Package Thermal Resistance	Junction to board thermal resistance (ThetaJB)		7		K/W
	Junction to ambient thermal resistance		23		K/W

4.3 Recommended Operation Conditions

Names	Descriptions	Min.	Typ.	Max.	Unit
VIN	Supply input voltage	4.5		60	V
V_{LEDn}-V_{LEDn-1}	Input voltage per channel			20	V
$I_{FET(DC)}$	Switch continuous current		1.0	1.5	A

4.4 Electrical Characteristics

V_{IN} = 14V, For digital outputs, C_{LOAD} = 20pF (Unless otherwise noted).

Parameter	Conditions	Min.	Typ.	Max.	Unit
I_Q	Consumption current from VIN (No switch and no communication) VLEDn=0V		5		mA
	Consumption current from VIN VLEDn=10V		2		mA
Current consumption during ELINS communication	12 channels work in Smart Mode with 244Hz PWM frequency while ELINS communication		8		mA
Startup time			2		ms
Charge pump					
Switch frequency	From auxiliary clock		5.0		MHz
$V_{chg\ pump}$	Voltage between CPP4 to LED12, CPP3 to LED9, CPP2 to LED6, CPP1 to LED3		7.8	9.4	V
I_{chg_pump} current capability of each charge pump from V_{CPPn}	At 27℃	200			μA
Charge pump consumption for LEDn	Zero load current		720		μA
LDO VDD5P0					
Output voltage		4.5	5	5.5	V
Load current			45	60	mA
Decoupling capacitor		2.2	4.7		μF
Clocks					
System clock frequency	Divided from system oscillator		10		MHz
System clock accuracy	After ELINS calibration, depends on the ELINS host	-0.25		+0.25	%

Parameter	Conditions	Min.	Typ.	Max.	Unit
Auxiliary clock frequency	Used for charge pump and watchdog		5.0		MHz
Auxiliary clock spread spectrum frequency range	Optional, range in room temperature	-8		+8	%
UVLO/POR/BOR					
VIN (UVLO rising)	UVLO rising threshold, VIN rising		4.1		
VIN (UVLO falling)	UVLO falling threshold, VIN falling		4.0		
VDD5P0 POR (rising)	VDD5P0 POR rising threshold, VDD rising, VIN=5V		2.8	4.0	V
VDD5P0 POR Hysteresis(falling)	VDD5P0 POR falling threshold, VDD falling, VIN=5V	2.0			V
BOR VDD1P5 (rising)			1.3		V
BOR VDD1P5 Hysteresis(falling)			100		mV
Temperature Sensor					
Accuracy of T_{JT}(adc)	Junction temperature read accuracy, returns the internal sensor voltage drop. The junction temperature must be calculated with MCU master	-10		+10	℃
T_{OT}	Over temperature warning, 3-bit configurable, and the default value of **TS_CFG** is 3'b000		160		℃
Over temperature warning threshold range	3-bit configurable, 10℃ for each step	90		160	℃
Accuracy of T_{OT}		-10		+10	℃
Watchdog Timer					
Timeout range	3-bit register configurable	8		1048	ms
ADC					
Resolution	Include sign bit for ADC1 and ADC2		12		bits
	Single-ended measurement for positive signal		11		bits
V_{ref}	Internal 2.4V reference voltage for ADC		2.425		V
Available mux channels	Temp sensors of 4 blocks, ADDR0 and 2 ADC input pins		8		

Parameter	Conditions	Min.	Typ.	Max.	Unit
ENOB	Effective number of bits		9		
T_{conv}	ADC conversion time			20	μs
PWM Dimming					
Resolution			12		bits
Accuracy of PWM Frequency	F_{PWM} config=244	240	244	248	Hz
	F_{PWM} config=488	480	488	496	Hz
MOSFET control					
$R_{DS(on)\_MOS}$	$R_{DS(on)}$ per switch, **NOT include** bonding wire	90	170	340	mΩ
R_{wire}	Resistance of bonding wire for each channel		60		mΩ
$R_{DS(on)}$	$R_{DS(on)}$ per switch, **include** bonding wire	130	230	400	mΩ
$R_{DS(on)\_3LEDs}$	$3R_{DS(on)\_MOS}+R_{wire}$		570		mΩ
Slew rate control					
$t_{RISE1(LEDn)}$	I_{LED} = 400 mA and VLED = 3.5 V. t_{RISE}: time for VDS to change from 10% to 90%. Register setting: Fastest(11)		1.0		μs
$t_{FALL1(LEDn)}$	I_{LED} = 400 mA and VLED = 3.5 V. t_{FALL}: time for VDS to change from 90% to 10%. Register setting: Fastest(11)		1.0		μs
$t_{RISE2(LEDn)}$	I_{LED} = 400 mA and VLED = 3.5 V. t_{RISE}: time for VDS to change from 10% to 90%. Register setting: Fast(10)		2.0		μs
$t_{FALL2(LEDn)}$	I_{LED} = 400 mA and VLED = 3.5 V. t_{FALL}: time for VDS to change from 90% to 10%. Register setting: Fast (10)		2.0		μs
$t_{RISE3(LEDn)}$	I_{LED} = 400 mA and VLED = 3.5 V. t_{RISE}: time for VDS to change from 10% to 90%. Register setting: Medium(01)		4.0		μs
$t_{FALL3(LEDn)}$	I_{LED} = 400 mA and VLED = 3.5 V. t_{FALL}: time for VDS to change from 90% to 10%. Register setting: Medium(01)		4.0		μs
$t_{RISE4(LEDn)}$	I_{LED} = 400 mA and VLED = 3.5 V. t_{RISE}: time for VDS to change from 10% to 90%. Register setting: Slow(00)		14		μs

Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{FALL4(LEDn)}$	I_{LED} = 400 mA and VLED = 3.5 V. t_{FALL}: time for VDS to change from 90% to 10%. Register setting: Slow(00)		14		μs
Phase shift control					
Phase shift configurable range	2-bit register configurable	64	256	341	Clock
Protection					
Switch-CHx OC threshold range	2-bit register config for open channel threshold.	6	12	21	V
OC detection Time	Response time of LED channel open detection.		100		ns
Switch-CHx SC threshold	LED channel short protection		1		V
Switch-CHx SC deglitch time	2-bit register configurable	32	128	256	μs
Charge pump output error detect	Charge pump error detect threshold (V_{CPPn}-V_{LEDn}), falling		3.8		V
	Charge pump error detect threshold (V_{CPPn}-V_{LEDn}), rising		4.1		V
Communication					
ELINS baudrate configurable range	Baud rate of ELINS, register **PRESCL**, 3-bit configurable	31.25		1000	kbps
IO interface					
V_{IH}	High-level input voltage threshold (RX, ADDR0, ADDR1, ADDR2, LP_MD)	2		VDD5P0 +0.3	V
V_{IL}	Low-level input voltage threshold (RX, ADDR0, ADDR1, ADDR2, LP_MD)	-0.3		0.8	V
I_{OH}	High-level output current (TX, LP_MD), [PDRV1:PDRV0]=00, VOH=VDD5P0-0.8 V	4			mA
	High-level output current threshold (TX, LP_MD), [PDRV1:PDRV0]=01, VOH=VDD5P0-0.8 V	8			mA
	High-level output current threshold (TX, LP_MD), [PDRV1:PDRV0]=10, VOH=VDD5P0-0.8V	12			mA
	High-level output current threshold (TX, LP_MD), [PDRV1:PDRV0]=11, VOH=VDD5P0-0.8V	16			mA

Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{OL}	Low-level output current (TX, LP_MD) [PDRV1:PDRV0]=00, V_{OL}=0.5V	4			mA
	Low-level output current (TX, LP_MD) [PDRV1:PDRV0]=01, V_{OL}=0.5V	8			mA
	Low-level output current (TX, LP_MD) [PDRV1:PDRV0]=10, V_{OL}=0.5V	12			mA
	Low-level output current (TX, LP_MD) [PDRV1:PDRV0]=11, V_{OL}=0.5V	16			mA
R_{TX}	Resistance from TX1 to TX2		10		Ω
R_{RX}	Resistance from RX1 to RX2		10		Ω
I_{IH}	Input leakage current (RX, ADDR0,ADDR1, ADDR2, ADC1, ADC2, LP_MD,TX) V_{VDD5P0}=5.5V, V_{PIN}=5.5V	-1		1	μA
MTP					
Junction Temperature TJ	for normal operation	-40		150	℃
	for programming/erasing operation	-40	125	150	℃
Endurance	At 125℃	1000			cycles
Data retention	At 125℃	10			years
Access time T_{ac}	one line	0.08	1		μs
Program time T_{pgm}	one bit	50		55	μs
Erase time	the whole MTP	180		202	ms

Note:

(1) Electrical Characteristics are valid over the full temperature range of Tj = -40℃ to +125℃ and a supply range of 6V ≤ VIN ≤ 60V unless otherwise noted.

(2) Guaranteed by design only, not tested during manufacturing.

5 Feature Description

5.1 General Operation

The iND83080 is a matrix controller aimed at pixel level LED lighting array management. Each LED light or LED lights group of the array is controlled by closing or opening the switches integrated in the iND83080. Using this strategy, the matrix lighting system can illustrate various pictures and marks, offering practical functions under real road vehicle operation circumstances.

The device communicates with host MCU through ELINS, which is a private protocol ELINS based on UART with advanced data structure to enhance robustness and functionality. The host can also control more than one device with different device ID. The device ID can be set by addressing pins. Warnings and errors from each device can also be sent to host by ELINS. The high frequency system clock integrated in iND83080 makes multi-devices synchronization possible. The short gap time between each rise edge of system clock ensures little error when different devices try to synchronize a same data frame of the host command.

A Nonvolatile Multi-Time Programmable Memory (MTP) is available for customers in the iND83080. MTP can store fixed regular operation information. It can be programmed to change default values of some registers. Once it's used and work in Smart Mode, software work is simpler and the communication with host MCU is less busy. In case of safety mode, custom information can be configured in register **DEFWIDTHx** in MTP Limp-home Mode default setting to make sure that when the device is out of master's control, it will work as the way customer wishes.

There are 4 groups of switches in iND83080. Each group includes 3 independent NMOS type switches. Each NMOS has a slew-rate adjustable driver, an over-voltage monitor and a short circuit monitor. An LED or LED group should be parallel connected with every switch, so that the device can control the lighting matrix correctly and safely. The 4 groups of switches support both series connection and parallel connection. When parallel connection is used, relative registers should be configured to avoid unsynchronized over-voltage or short circuit protection.

Each switch is controlled by 12-bit Pulse Width Modulation (PWM), the width and frequency of which are configured by register setting. In addition, the phase shift of the PWM waveform is configurable, so the cooperation of different switches is realized to avoid current spike.

All NMOS switch drivers need power supply rail higher than the voltage of the corresponding V_{LEDn} in one of the 4 groups. To correctly supply the internal circuit, 4 charge pumps are integrated in iND83080, each serves one group of switches. Each charge pump's output pin should connect a decouple capacitor to the LEDn pin placed next to it. For safety concern, the voltage between the charge pump's output and the relative LEDn is continuous monitored. Once the voltage difference is lower than the threshold voltage, an error flag is sent to host for warning.

The driving clock source of charge pump is the always-on auxiliary clock. For EMI optimization, this clock has spread spectrum function, which will periodically change the clock's frequency. This auxiliary clock is also used in start-up state machine control modules and the watchdog.

When a switch is closed to bypass the external LED, large current flows through the switch, which leads to temperature rise. To avoid over-temperature operation, 4 temperature monitors are distributed close to 4 NMOS switch groups, respectively. Each temperature monitor focused on a group has independent warning flag. Once the temperature of any group is high than the configured threshold, iND83080 sends the corresponding temperature warning flag to the host.

The signal from internal temperature sensor is also measured by an internal ADC. This ADC will

monitor the junction temperature and record it in relative registers. Meanwhile, the ADC can monitor off-chip voltage signal of the ADC1 and ADC2 pin, and records the voltage information in registers, too. Additionally, ADDR0 is one of the ADC channels, lower 3 bits Device ID value is determined by highest 3 bits of ADDR0's sample value, in which the ADDR0 should tie to resistors divider between VDD5P0 pin and GND, which makes sure that the iND83080 supports multi-device application up to 32 devices.

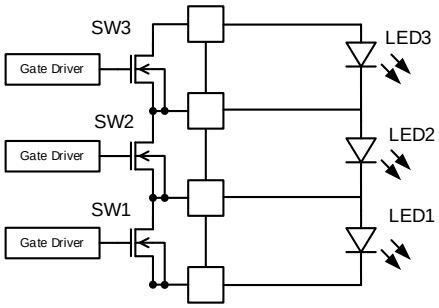
The VDD5P0 pin is the output of an internal 5V LDO with input voltage up to 60V, which means it can connect to 12V vehicle battery directly. This LDO is part of Power Management Unit (PMU). Apart from this, the PMU includes a core LDO supplying 1.5V power rail to digital core, a bandgap reference, Power-On Reset (POR), Brown-Out Reset (BOR), and Under Voltage Lock Out (UVLO).

In general, the iND83080 is a highly integrated matrix controller with multi-dimension protection, and is suitable for customized design and different applications of vehicle exterior lighting system.

5.2 Internal Switch Resistance Analysis

The internal switch (connected between LED_n and LED_{n-1}) has a measurable typical $R_{DS(on)}$ value of 220mΩ, which includes the resistance of the two internally-connected bond wires. Meanwhile, the on-resistance of the 3×seried-connected switches ($R_{DS(on-3LEDs)}$) is not simply the number of channels multiplied by 255mΩ because there are not two conducting bond wires for every series connected switch, it is $3*R_{DS(on)}+R_{wire}$ and the typical value of it is about 595mΩ. The calculation method is same for other different multiple series connected switches.

The dominant power loss mechanism in the device is the I^2R loss through the switches. It is important to note that the power dissipation is PWM duty cycle dependent. When the duty cycle of PWM dimming is D, the effective resistance of power loss is (1-D) * $R_{DS(on)}$.



5.3 Power Management Unit

5.3.1 Power Supply

The iND83080 can withstand wide voltage transients that exceed their nominal voltage during load-dump and cold-crank conditions due to its internal wide input range (up to 60V) PMU block. Specifically, the PMU block includes:

1. Main LDO: it is an always-on block and regulates the voltage from VIN to 5.0V. The output pin of main LDO is VDD5P0 and it needs a 2.2μF off-chip capacitor. Meanwhile, the main LDO has internal output over current limit protection, so that it can get stronger robust when start-up. Most of analog blocks are powered by the main LDO, and the internal POR_VDD5P0 block detect the voltage level of VDD5P0, if it exceeds POR threshold, internal POR signal will release and the power-up sequence detection will be active.
2. Bandgap: the internal high-precise bandgap is used for ADC and other detection blocks as voltage or bias current reference.

3. VDD_1P5: there is a capless LDO on the device, which regulates the voltage from VDD5P0 to 1.5V as the power supply of digital part. This LDO will start-up after both UVLO and POR_VDD5P0 are released, and if the output of the LDO exceed BOR's threshold (typ.=1.35V and it is register configurable), the BOR signal will be released and digital control core will be active.

5.3.2 UVLO Detection and Protection

When VIN voltage is below UVLO threshold voltage (4.0V typ.), the digital core unit stays in reset status and communication is not enabled. If VIN is recovered above the UVLO threshold voltage, the state-machine will be active after deglitch of 2ms. If the status is ok after a full power up system diagnosis, device allows the communication work well again.

5.4 Clock and Reset System

5.4.1 System Clock

There is a high frequency oscillator integrated, the output of which is affected by the process variation, supply voltage and ambient temperature, which results in ±5% frequency variation.

During ELINS communication, the device oversamples the high frequency clock to synchronize and calibrate the system clock. The variation of synchronized clock will less than ±0.25% with the host.

5.4.2 Auxiliary Clock

Another clock with spectrum spread function is integrated in this device to drive charge pump and watchdog timer. Some low frequency state machine control circuits also operate under this clock. This clock is more dependent on supply voltage and ambient temperature. There also exists a trimming system to fix the process drift.

In order to minimize the electro-magnetic field the charge pump spreads, this clock has a spectrum spread function, which is about ±8% frequency variation with 5-bit resolution configured in register **SEL_SSC_STEP** in MTP. The default SSC frequency is 10.7kHz.

5.4.3 Reset Management, POR and BOR

The device integrates Power on Reset (POR) circuitry for LDO VDD5P0 and Brown Out (BOR) block for internal LDO VDD1P5. POR monitors the main 5V output LDO supply and generate a reset every time supply voltage is power up. Both maintain their output reset active if the monitored supply voltage is not above the minimum supply level to ensure safe operation of the device. In case any POR or BOR is triggered, the device can be configured to either do the following:

- Control logics are turned to reset state
- All the registers are reset to default value

Meanwhile, Control logics and registers can be manually reset by setting 1 to corresponding register listed below:

REQ_SOFT_RSTN: Set 1 to trigger a soft reset of device
REQ_MTP_RSTN: Set 1 to trigger a soft reset of MTP module
REQ_PWM_RSTN: Set 1 to trigger a soft reset of PWM module
REQ_ELINS_RSTN: Set 1 to trigger a soft reset of ELINS module
REQ_ADC_RSTN: Set 1 to trigger a soft reset of ADC module

5.5 Charge Pump

Four charge pumps are integrated inside this device. Each of them is used in a switch group with 3 NMOS switch and drivers. The internal charge pump can output voltage roughly 7.8V higher than V_{LEDn} to supply the driver circuit of switch NMOS. In this way, the gate to source voltage of NMOS switches can be driver to 5V, which means the switch resistance is minimized.

When the V_{LEDn} changes rapidly from high voltage to lower than 5V, a short time of reversed current exists from HVDD to VDD. If 1μF capacitor is used at the VDD pin, the voltage will increase about 8mV before LDO reacts to this extra charge.

If the voltage difference between V_{CPPn} and V_{LEDn} of anyone of the 4 charge pumps is lower than 3.8V(typical threshold), the warning flag in **PMUA.FLAG_VCPP_ERROR** will be set high to indicate connection error of off-chip capacitor, respectively. Both open circuit or short circuit connection may cause this warning.

A 100nF capacitor of at least 10V voltage stress level is required between the V_{LEDn} and charge pump output V_{CPPn} for stability and ripple reduction.

5.5.1 Charge Pump Fail-safe Operation

If the voltage difference between V_{CPPn} and V_{LEDn} is lower than 3.8V(typical threshold), the warning flag in **PMUA.FLAG_VCPP_ERROR** will be set high to indicate charge pump failure. There are two possible failures. First, if the V_{CPPn} is shorted to the closest V_{LEDn} pin, the flag will be set high; Second, if the NMOS driver circuit consumes large current from the charge pump, the flag will be set high. It should be noted that, if the external capacitor of charge pump is open circuit, this flag will mostly not be set high. However, under this circumstance, the voltage of V_{CPPn} would oscillate due to stability problem. This flag generator only works when the V_{IN_UVLO} releases. If V_{IN_UVLO}=1, this flag signal maintains 0.

5.6 LED Switch Faults Detection

5.6.1 LED Open Channel Protection

An internal comparator monitors the drain-to-source voltage of the internal switch during LED is on, if the voltage exceeds the programmable threshold voltage of V_{TH-O}, the device overrides will turn on the switch immediately. When an Open Channel event is detected, the PWM switch is closed and an error bit set. This process allows the device to bypass this LED and the other LEDs to continue to operate. This action allows current flow in the rest of the LED string in the presence of a faulty or damaged LED, and protects the internal switch from surge voltage. The internal latch holds this state until a subsequent LED turn-off event. The protection circuit also sets the corresponding bit in register **SYSCTRLA.FLAG_OV**.

The device allows another OV fault recovery configuration. If the register **SYSCTRLA.FLAG_OV**=1 the system recovers automatically when clearing the fault flags (by writing **SYSCTRLA.CLR_OV**=1) rather than the next LED turn-off event.

The open channel threshold voltage, V_{TH-O}, can be programmed independently for each LED sub-block (3×series-connected switches) via a 2-bit value in the corresponding register **OV_BxCFG** in MTP. The programmable threshold helps applications where multi-chip LEDs with higher forward voltage drops are used. Furthermore, in applications where significant ringing occurs during switching events that may result in an undesired over-voltage triggering, higher OVLMT thresholds can help mitigating the problem.

When the device is configured as described in section Parallel Switch Setting, digital circuitry of the device turns on all of the corresponding switches, if one of the parallel switches detects an over voltage condition. This allows all of the paralleled switches to share the shunted current instead of only a single switch handling the full LED current.

5.6.2 LED Short Channel Protection

When LED is ON, LED short is also detected through monitoring the drain-to-source voltage of the internal switch during PWM regulation. If the voltage does not exceed the V_{TH-S} threshold after deglitch when internal switch is OFF, the corresponding bit in register **SYSCTRLA.FLAG_SC** register is set to 1. The MCU can determine whether to bypass the channel or not, and clear the fault bits in the **SYSCTRLA.FLAG_SC** register by writing a 1 to the **SYSCTRLA.CLR_SC**, provided that the corresponding fault input is no longer active. SC fault blanking time can be configured by 2-bit register **SYSCTRLA.SEL_SC_DGH**, to meet different switch slew rate and avoid unwanted error flag.

5.7 LED Switch Operation

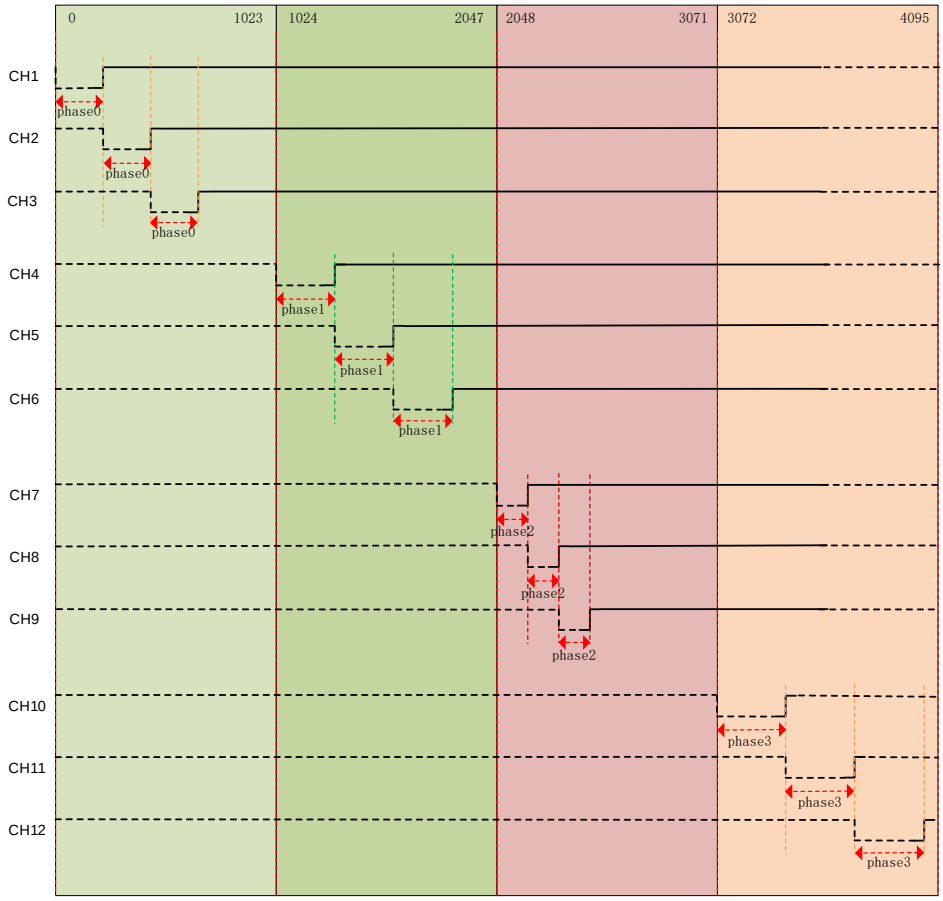
5.7.1 Switch Slew Rate Control

The slew rate of switching process can be programmed. Different slew rate setting corresponds to different switch pre-driver output capability, so the rising and falling speed of the gate-source voltage of a single switch is controlled. As a result, the rising and falling speed of PWM edge at VLEDn will change accordingly. There are totally 4 level of slew rate speed configured by 2 bits register, which are fastest level, fast level, medium level, and slow level. Every one of the 4 switch groups' slew rate can be set individually in register **SR_BxCFG** in MTP, respectively.

5.7.2 PWM Phase Shift

An internal logic of PWM phase shift for each channel is realized in the device, which claims the difference between the transition time of LED ON-to-OFF. The phase shifts of 12 channels are fixed to a certain value, determined by register **PWM.FPHASE_SEL**, as illustrated in the following table:

Channel	FPHASE_SEL=0	FPHASE_SEL=1	FPHASE_SEL=2	FPHASE_SEL=3
PHASE0	64	128	256	341
PHASE1	128	256	512	682
PHASE2	192	384	768	1023
PHASE3	1024+64	1024+128	1024+256	1024+341
PHASE4	1024+128	1024+256	1024+512	1024+682
PHASE5	1024+192	1024+384	1024+768	1024+1023
PHASE6	2048+64	2048+128	2048+256	2048+341
PHASE7	2048+128	2048+256	2048+512	2048+682
PHASE8	2048+192	2048+384	2048+768	2048+1023
PHASE9	3072+64	3072+128	3072+256	3072+341
PHASE10	3072+128	3072+256	3072+512	3072+682
PHASE11	3072+192	3072+384	3072+768	3072+1023

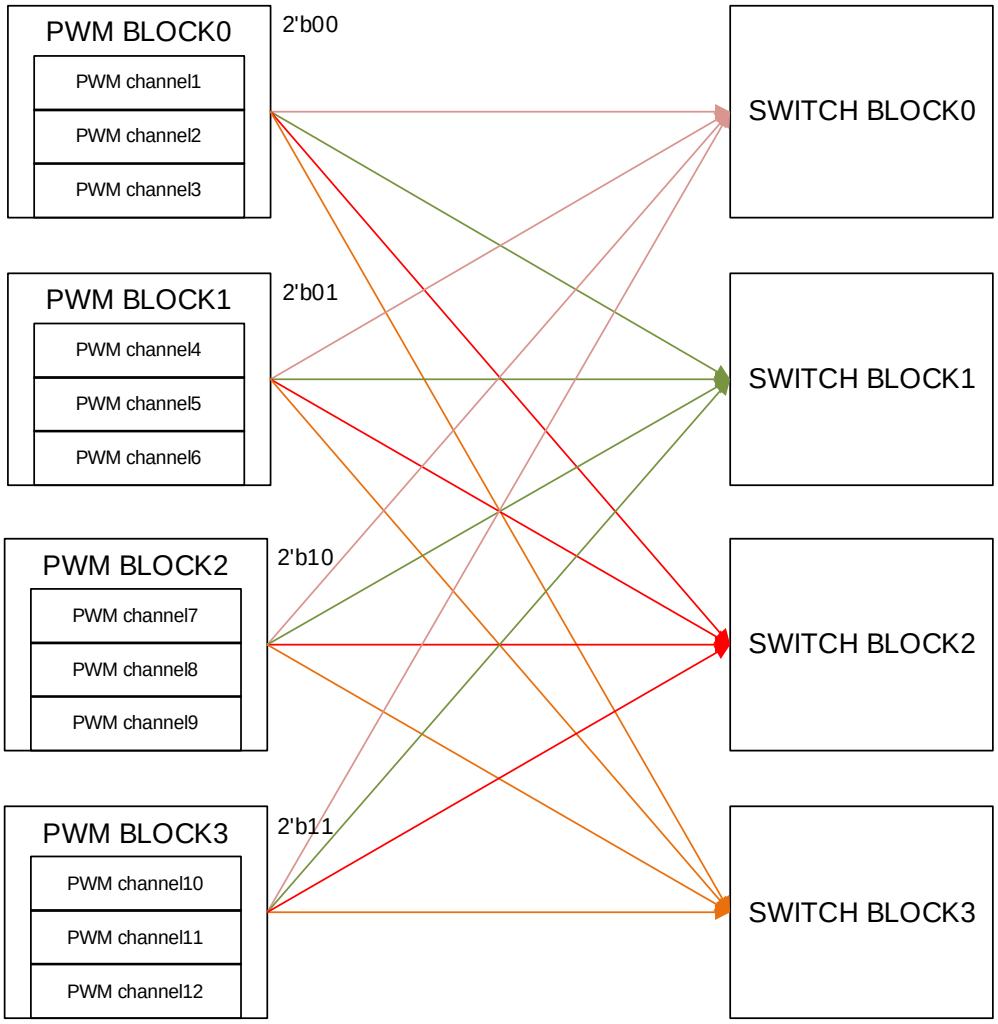


The 12-bit PWM dimming results in a PWM counting of 0~4095. The LED of each channel is turned off only when the PWM counter equals to the corresponding value in the table during ON status. Meanwhile, it will remain off during OFF status.

The primary benefits of the different phase shifts can be concluded as following:

1. When 12 LEDs are connected in series, a risk occurs when some of them are turned off at the same time, resulting in a large inrush current flowing back to internal driver switches. This may make the switch(es) burned out and broken down.
2. The Electro-Magnetic-Interference (EMI) concerns can be mitigated, by spreading the LED transition/phase times of the 12 channels within each PWM cycle. At transition, the temporal derivations of LED voltages and currents are usually maximal and easier to lead to a significant radiation, which degrades the EMI tolerance. By spreading them, all the radiation peeks are staggered, and therefore the interferences are not so concentrated and makes the EMI tenderer.

5.7.3 Parallel Switch Setting



In order to reduce the channel switch resistance, the iND83080 supports to parallel configuration for each group. The switch group, which contains 3 switches and shown in right side of diagram, can be assigned to four different PWM blocks as left side of diagram based on 2 bits registers. When switch blocks are used in parallel, the 2bits PWM block selection settings **SEL_PWM_SWx** in MTP must be configured to be the same value so that they can turn on at the same instant and use the same PWM information. For example, in typical single device application, if we want to parallel channels LED7-LED9(PWM block2) with channels LED1-LED3(PWM block0), we need to set **SEL_PWM_SW2** = 0, and the PWM regulation parameter will be taken over by PWM block0's registers.

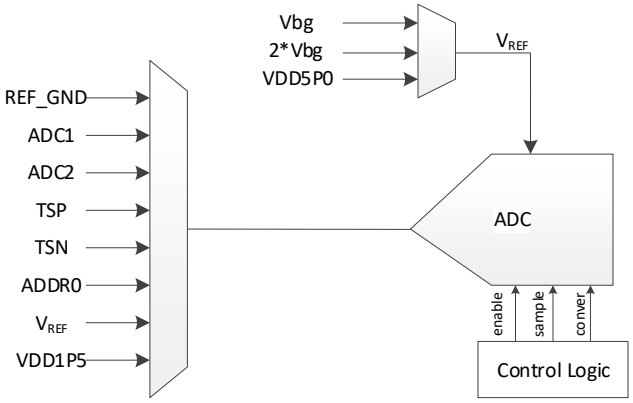
5.8 Analog-to-digital Converter

5.8.1 ADC Operation and Work Mode

The Analog-to-digital Converter (ADC) features a Successive-Approximation ADC(SAR) in single-ended mode, with a sampling rate up to 250 kSps. The ADC is connected to an 8-channel analog multiplexer, which allows eight single-ended voltage inputs. The single-ended voltage inputs refer to 0V (GND). The ADC input channel can either be internal or external through the analog input pins. The reference voltage for the ADC is selectable.

- 11-bit resolution in single-ended mode
- Up to 250 kSps

- Up to 8 multiplexed single-ended input channels
- 0V(GND) to VDD5P0 ADC input voltage range
- Multiple internal ADC reference voltages



5.8.2 Temperature Sense

The temperature protection is necessary, due to the high power dissipation from power NMOS groups. There are 4 remote sense subblocks, each of them is located close to one power NMOS group. Therefore, it is possible to separate over-temperature information of different switches to accurately position the high temperature area.

There is only one comparator used to output over temperature flag. The 4 remote sense circuits will be connected to the comparator at different time. The over-temperature flags of 4 subblocks are recorded in register **STS_OTx**, respectively.

The over temperature threshold can be changed by changing the current through the register. There are 3 bits modulation used to change the threshold from 90℃ to 160℃ in register **TS_CFG** in MTP. The output voltage of remote sense will be sent to ADC to sample the temperature information for further process.

The over-temperature protection module works only when the corresponding remote sense subblocks output voltage is sampled by the ADC and compared in the over-temperature comparator. Normally the ADC samples the voltage and gets all four switch blocks temperature statuses and ADC sampling data at one trigger. In order to protect all switches at all time, ADC sampling need to be refreshed continuously and the over temperature flag is to be monitored.

To sample the temperature remote sense subblocks output voltage, two of ADC channels must be assigned to TSP and TSN simultaneously to sample temperature of subblocks. The 4 subblocks voltage are sampled one by one and conversion result that generated from ADC are output to register **ADC_DATAx.DATAy**.

Given $\Delta_V = TS_P - TS_N$ in a subblock, the ambient temperature will be

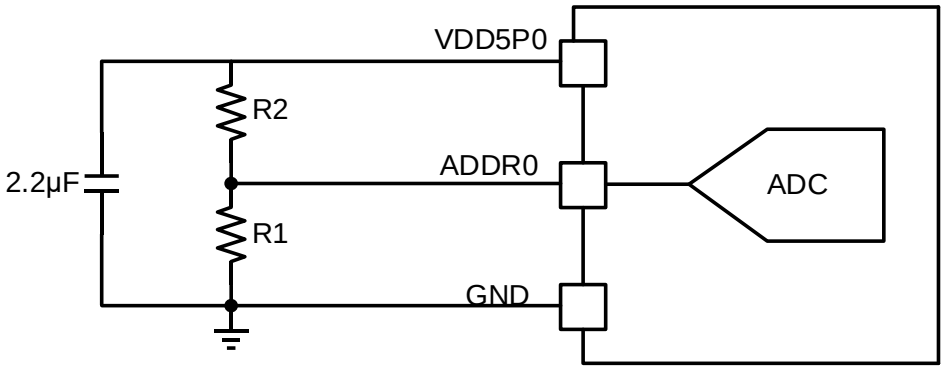
$$T_{SNS} = \frac{\Delta_V - 108.675mV}{400uV}$$

T_{SNS} is the ambient temperature (by Centigrade).

5.8.3 Device Address Setting

As the ADC's block diagram described, the ADC can be used to set the device address. The device address is determined by ports ADDR2, ADDR1, ADDR0. When register **ADDR_MODE** in MTP bit is set to "0", ADDR1 and ADDR2 are digital inputs (need tie to GND or VDD5P0), while ADDR0 is connected to an analog voltage divided from VDD5P0. The ADC converts this voltage with an

average of 32 times sampling, and takes the most significant 3 bits as the least significant 3 bits of the device address. Combined with ADDR2 and ADDR1, up to 32 devices can be connected in a single bus in this mode.



DEV_ID[4]	DEV_ID[3]	DEV_ID[2]	DEV_ID[1]	DEV_ID[0]
ADDR2	ADDR1	ADC_DATA[10]	ADC_DATA [9]	ADC_DATA [8]

The diagram of ADDR0 connection is shown as above.

DEV_ID[2:0]	V_ADDR0(V)		
	min.	typ. (1)	max.
000	0(1)	0.063*VDD5P0	0.125*VDD5P0
001	0.125*VDD5P0	0.188*VDD5P0	0.25*VDD5P0
010	0.25*VDD5P0	0.313*VDD5P0	0.375*VDD5P0
011	0.375*VDD5P0	0.438*VDD5P0	0.5*VDD5P0
100	0.5*VDD5P0	0.563*VDD5P0	0.625*VDD5P0
101	0.625*VDD5P0	0.688*VDD5P0	0.75*VDD5P0
110	0.75*VDD5P0	0.813*VDD5P0	0.875*VDD5P0
111	0.875*VDD5P0	0.938*VDD5P0	VDD5P0(2)

Note:

1. The corresponding voltage values for each DEV_ID are given as above, A resistor divider between VDD5P0 and GND is recommended to reach the specific voltage. The total resistance value should be greater than 10kΩ for power optimization.

When using 5-bit Device ID mode, the ADDR0 pin could be tied to VDD5P0 or GND to indicate 111 or 000. Detailed table is shown below.

Connection(5-bit Mode)			Device ID		
ADDR2	ADDR1	ADDR0	Bin.	Dec.	Hex.
L	L	GND	0b00000	0	0x00
L	L	VDD5P0	0b00111	7	0x07
L	H	GND	0b01000	8	0x08
L	H	VDD5P0	0b01111	15	0x0F
H	L	GND	0b10000	16	0x10
H	L	VDD5P0	0b10111	23	0x17
H	H	GND	0b11000	24	0x18
H	H	VDD5P0	0b11111	31	0x1F

Note:

1. The high level(H) and the low level(L) is defined in the Electrical Characteristics table.

Once the power-on reset is finished, the ADC starts to sample the ADDR0 voltage. Before the sampling process is completed, neither the device can communicate with a single write/read command nor a broadcast command can be sent to trigger the ADC sampling of the device address. The device supports 3-bit Device ID mode by writing 0x3 to register **ADDR_MODE** in MTP. Since the command takes effect immediately, it's highly recommended to be sent with Broadcast Write command (instead of Single Device Write command). In the mode, pin ADDR0 is a digital input channel. Detailed table is shown below.

Connection(3-bit Mode)			Device ID	
ADDR2	ADDR1	ADDR0	Bin.	Dec.
L	L	L	0b00000	0
L	L	H	0b00001	1
L	H	L	0b00010	2
L	H	H	0b00011	3
H	L	L	0b00100	4
H	L	H	0b00101	5
H	H	L	0b00110	6
H	H	H	0b00111	7

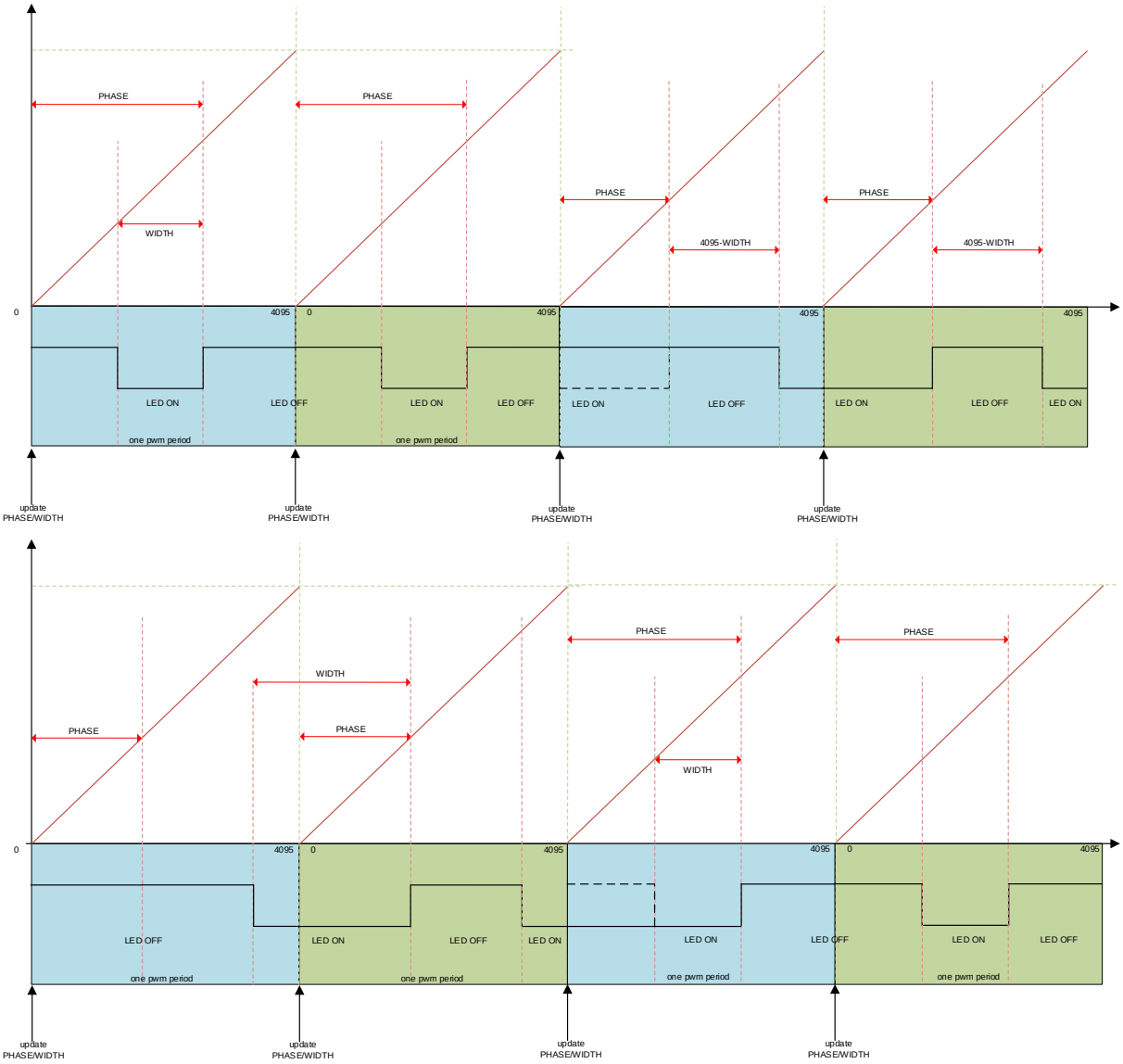
The bit **ADDR_MODE** is loaded from MTP after powering up automatically. Once MTP loading is finished, the ADC starts to sample the ADDR0 voltage (when **ADDR_MODE**=0). Before the sampling process is completed, neither the device can communicate with a single write/read command nor a broadcast command can be sent to trigger the ADC sampling of the device address.

5.9 Watchdog Timer

The watchdog timer (WDT) is primarily used to monitor the communication bus and driven by the auxiliary clock. The counter of watchdog timer is always reset to 0 after receiving a command with the correct CRC value, even if the device address is not matched. If communication frame on the bus is illegal or the bus keeps silent for a certain time, which is configurable by changing the register **WDT_BARIUM.TIMEOUT_SEL** and its default value is 1048ms, the device will enter the Limp-home Mode. During the Limp-home Mode, the watchdog timer is stopped.

5.10 Internal PWM Dimming

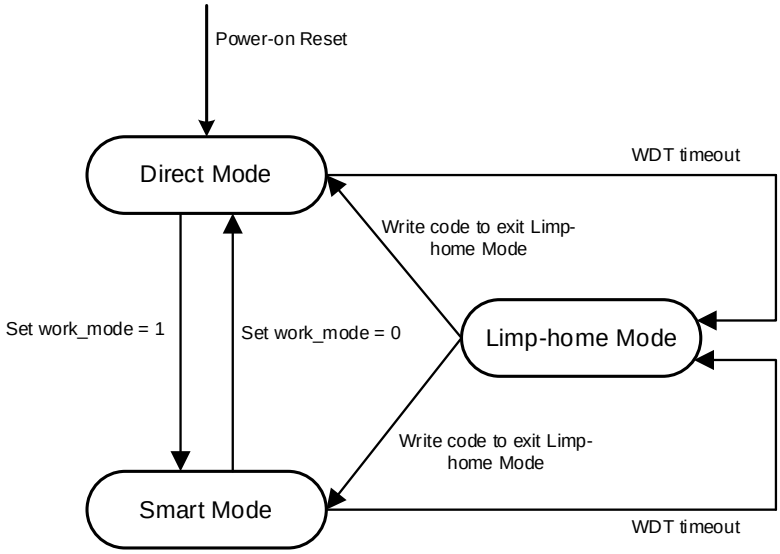
The iND83080 have an internal 12-bit resolution PWM generator module for each channel, which means the time accuracy is 1μs, at 244 Hz or 0.5μs, at 488 Hz application. The resolution in terms of PWM percentage is 0.024 %. The supported frequency range of PWM is from 222Hz (min) to 2.44kHz (max) and the frequency value can be set by register **PWM.PWM_FREQ_SEL**. The default PWM frequency is 488Hz. Each time the system is powered up, the PWM frequency value would be loaded from MTP.



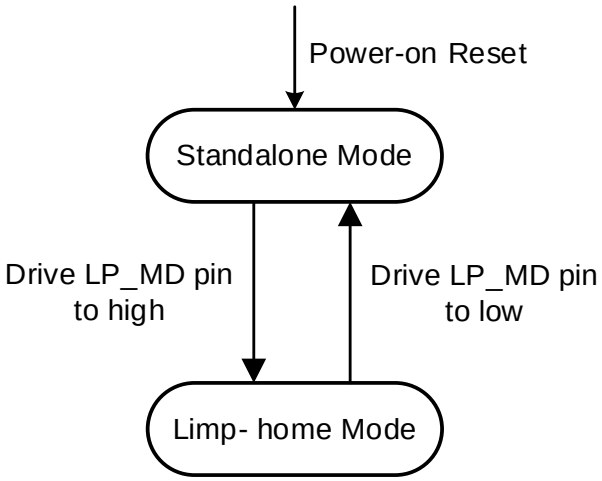
The PWM control signal is generated based on an internal counter from 0 to 4095. The initial status of PWM is set to “1”, which means the LED is OFF. If the **WIDTHx** value is equal to 0, it means the corresponding LED is always OFF and the status of PWM control signal is always set to “1”. The PWM level only changes from “0” to “1” when the counter is equal to **PHASEx**. Meanwhile, if the **WIDTHx** is equal to 4095, it means the corresponding LED is always ON and the level of PWM is always set to “0”.

If the **WIDTHx** value is equal to **PHASEx**, the PWM status changes to 0 when the counter is equal to “0”, and it triggers to “1” when the counter is equal to **PHASEx**. If the **WIDTHx** value is smaller than **PHASEx**, the PWM level changes to “0” when the counter value is equal to (**PHASEx**-**WIDTHx**), And it triggers to “1” when the counter is equal to **PHASEx**. If the **WIDTHx** value is larger than **PHASEx**, the PWM status changes to “1” when the counter is equal to **PHASEx**, and it trigger to “0” when the counter is equal to (4096+**PHASEx**-**WIDTHx**).

5.11 Function Mode



There are two working modes set by register when register **SEL_SAM_NORM** is 0 in MTP, the Direct Mode and Smart Mode is designed to work with ELINS bus to communicate with the master. If communication fault happens in Direct Mode and Smart Mode for a certain time, the device will enter Limp-home Mode automatically. The device will exit Limp-home Mode when receiving a Limp-home Mode deactivation code through communication bus.



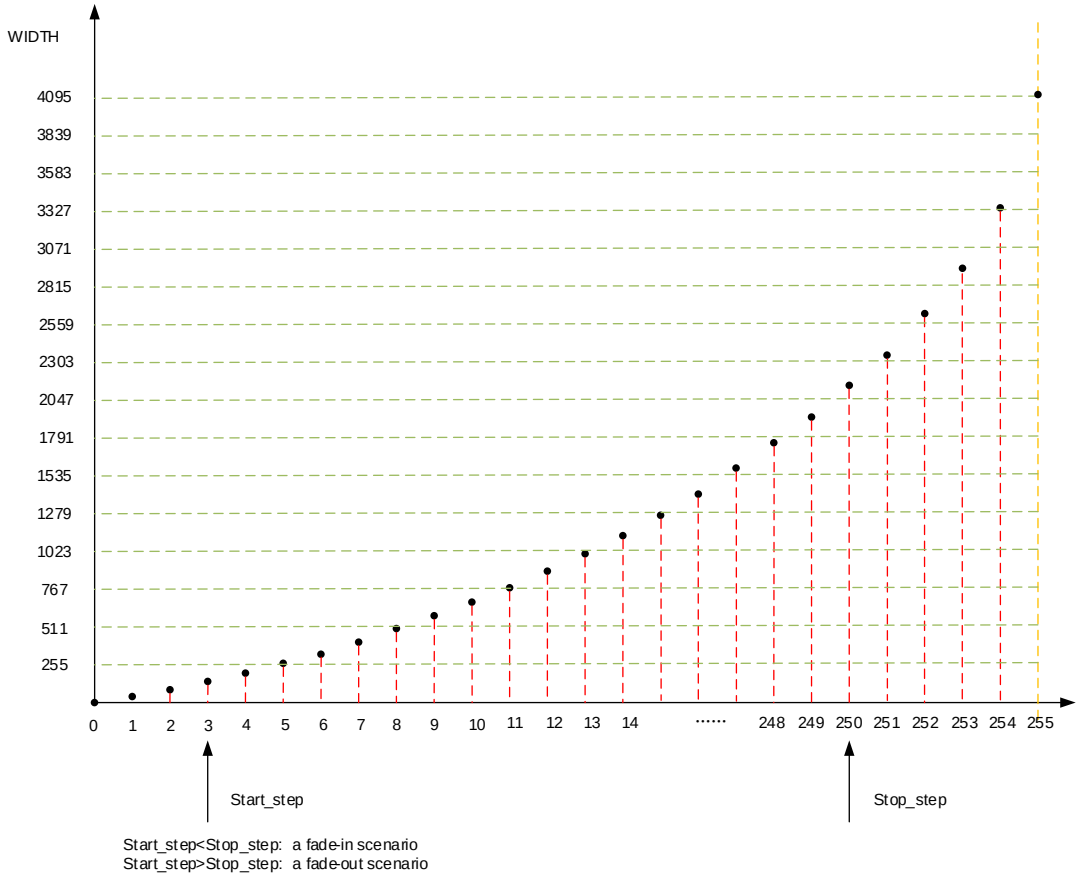
The device will enter the Standalone Mode when register **SEL_SAM_NORM** is 1 in MTP. In Standalone Mode, the LP_MD pin is used to trigger the Limp-home Mode.

5.12 Direct Mode

In Direct Mode, arbitrary PWM channels can be enabled by setting “1” to the corresponding bits of register **PWM.ENA_REQ**. Or write “1” to **PWM.ENA_REQ_ALL** to enable all 12 PWM channels simultaneously, while write “1” to **PWM.CLR_REQ_ALL** to disable all of them.
The brightness of each channel is determined by register **PWM.WIDTHx[11:0]** (x=0, 1, … ,11), with **PWM.WIDTHx[11:0]**=0x000 for fully turned-off of LEDs, and **PWM.WIDTHx[11:0]**=0xFFF for fully turned-on. An automatic updating occurs when the PWM counter rolls over.
To enter the Direct Mode, the register **SYSCTRLA.WORK_MODE** should be 0.

5.13 Smart Mode

In Smart Mode, the PWM width can be generated according to a third-order polynomial, whose coefficients define the PWM dimming parameters. It is very effective to reduce data traffic of serial communication. The diagram of PWM dimming curves in Smart Mode is shown as below:



It is described by a third-order polynomial. The third-order polynomial of Smart Mode is:

$$y(x) = k_3 * x^3 + k_2 * x^2 + k_1 * x + k_0$$

Here, k_3, k_2, k_1 are coefficients between $[-0.0625, 0.0625)$, k_0 is non-negative coefficient between $[0, 4095]$, x is the frame step number.

k_3, k_2, k_1 are stored in **Kn_CURx** as 13-bit fixed point numbers including sign bit (13Q16), which **Kn_CURx** between $[-4096, 4096)$ maps to k_n between $[-0.0625, 0.0625)$. k_0 is an unsigned 12-bit non-negative integer between 0 and 4095, which is **K0_CURx**.

In Smart Mode, Each Smart Mode channel controls the corresponding PWM waveform. All 12 channels can be configurated independently, which offers sufficient freedom in controlling the dynamic lighting play. Up to 8 PWM dimming curves are stored in MTP, whose coefficients are loaded after powering up. Each channel can choose one of them via setting register **SRTCHx0.CUR_SELx**.

SRTCHx1.START_STEPx and **SRTCHx1.STOP_STEPx** can be an arbitrary value between 0 and 255. This means the dynamic light play can start or stop at any point in the dimming curve. Set **SRTCHx0.NUM_DECIMx** between 1 and 31 to jump by several steps from start step to stop step, instead of moving only 1 step each time (**SRTCHx0.NUM_DECIMx** = 0 by default).

Write 1 to **SRTCHx0.PLAYx** to start the light effect on the corresponding channel. The LED of each

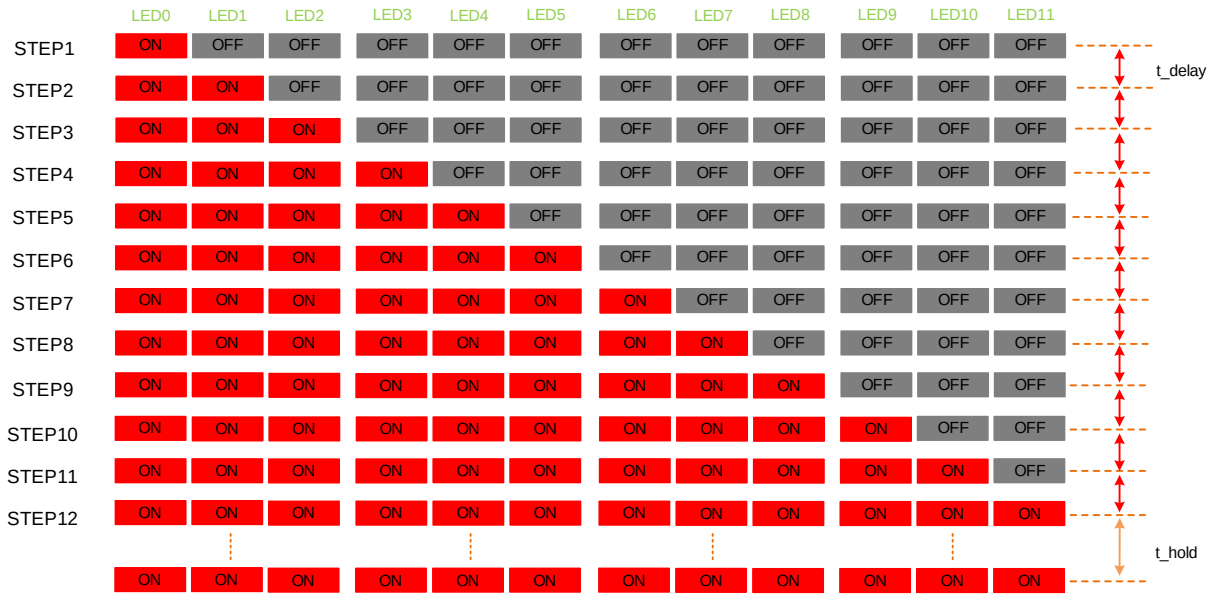
channel turns fully off after the curve finished. Respectively, the registers **SRTCHx0.NOWx** and **SRTCHx0.NXTx** indicates playing the next curve immediately or at the end of the current play. Additionally, you can add delay time and hold time before and after each curve play by setting registers **SRTCHx0.DELAY_TIMEUNIT_SELx**, **SRTCHx0.HOLD_TIMEUNIT_SELx**, **SRTCHx1.DELAYx** and **SRTCHx1.HOLDx** respectively. The first two registers determine the base time unit for delay and hold time, while the latter two are multipliers. Therefore, the delay and hold time are calculated as:

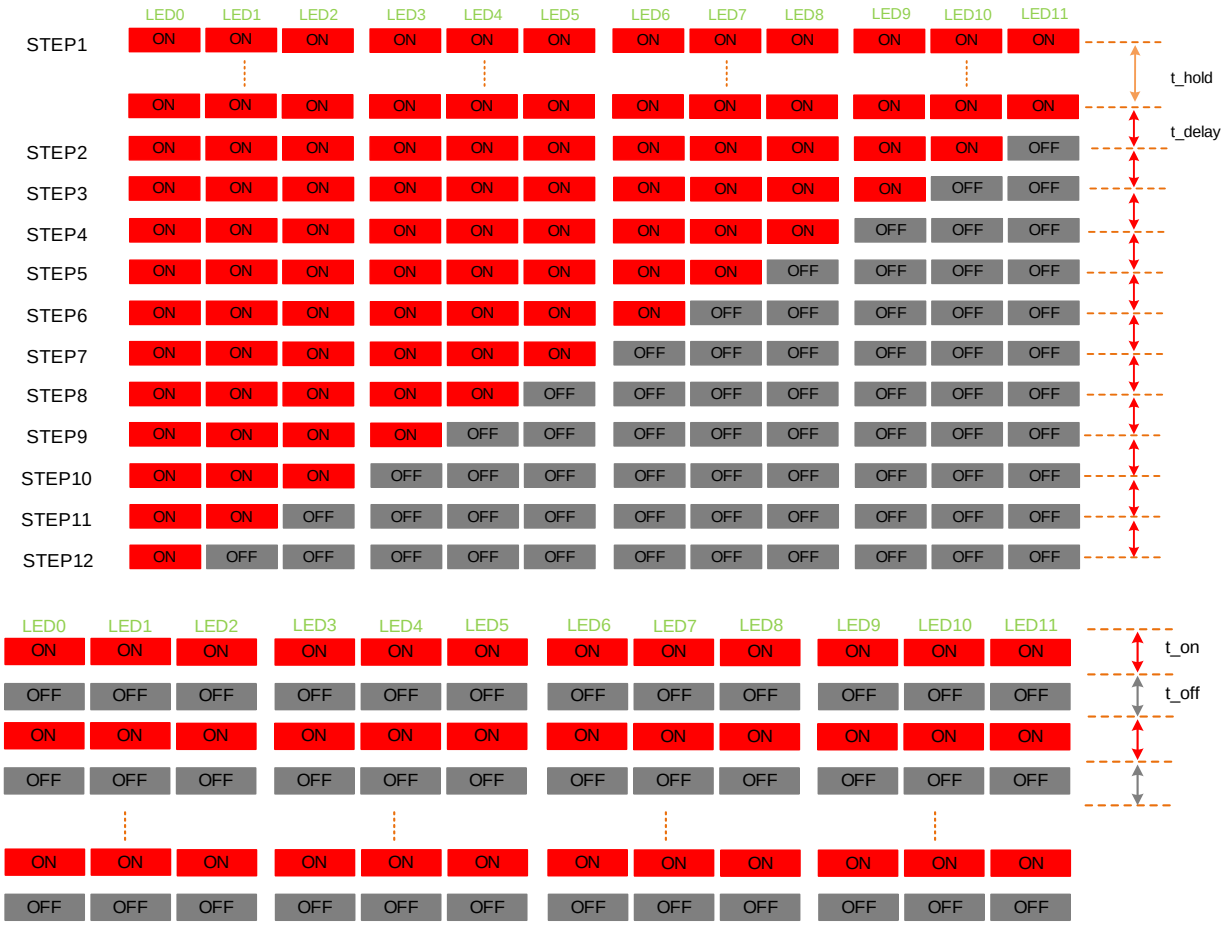
$$t_{delay} = DELAY\_TIMEUNIT\_SELx[3:0] \cdot DELAYx[7:0]$$
$$t_{hold} = DELAY\_TIMEUNIT\_SELx[3:0] \cdot DELAYx[7:0]$$

The register **SRTCHx0.STEP_PRDx** control the play speed defined by the duration of each step. To enter the Smart Mode, set register **SYSCTRLA.WORK_MODE** to 1. If the Limp-home Mode is triggered, the device will leave Smart Mode and enter Limp-home Mode. All light effect playback status in Smart Mode will be reset. The LEDs' brightness is set according to the Limp-home Mode configuration. After resuming from Limp-home Mode, the light effect should be start again.

5.14 Standalone Mode

The Standalone Mode is designed for no communication application scenario. The device can be configured into Standalone Mode by setting register **SEL_SAM_NORM** to 1 in MTP. Two lighting dynamic effects are supported: waterfall light and flashlight. They are controlled by hardware signal from GPIO's input electrical level or pulse trigger. The signal activity polarity can be set independently by setting register **PWM.POLAR_SIG_FAL** or **PWM.POLAR_SIG_WFL**. The playback effect and parameters are described below:





The PWM widths in Standalone Mode can be configured by setting register **SYSCTRLA.SAM_CFG_WIDTH**. During power on configuration, all Standalone Mode parameters will be loaded from MTP, so users can configure the lighting effect according to the market demand.

5.15 Limp-home Mode

When the device is working in Direct Mode or Smart Mode, barking of the watchdog forces the device into Limp-home Mode. In this case, to leave Limp-home Mode, follow the steps:

a) set the register **SYSCTRLA.DEACTIVE_LHM_CODE** to 0x9116

b) write “1” to the register **SYSCTRLA.DEACTIVE_LHM**

The LED brightness of each channel is configured by a default value of pulse width in register **PWM.DEFWIDTH** at once the device enters Limp-home Mode. When **PWM.DEFWIDTH** = 0x0, the LED turns fully off, while **PWM.DEFWIDTH** = 0xF, the LED turns fully on. The default width configurations are loaded from MTP after powering up.

5.16 LED Brightness Calibration Function

The device embeds an internal function for LED brightness calibration. It adjusts the brightness of each LED, driven by the same current, to the same level via setting the calibration register **CALI_BRIx[4:0]** in MTP to various values on each channel. They are loaded from MTP after powering up. The calibration formula is given:

$$p_{calibrated} = p_{original} \cdot (1 - CALI\_BRIx/128)$$

where p is the duty cycle. The calibration works in any circumstances, no matter the device is in Direct Mode, Smart Mode, Limp-home Mode, or Standalone Mode.

5.17 MTP

The device has a MTP (Multiple Time Programmable) memory. The system configuration data can be customized by users very easily and flexibly. After every power-up, the data will load from MTP automatically. The ELINS interface can launch an MTP erase/program operation and access the desired MTP register map. The parameters stored in MTP list below:

- MTP load enable code
- ELINS baud rate
- PWM frequency select
- Eight PWM dimming curve coefficients
- Twelve LED brightness calibration factors
- Twelve default PWM width used in Limp-home Mode
- SSC enable and step period
- Over-temperature threshold from 90~160℃
- LED over-voltage threshold for 4 block channels
- LED slew rate threshold for 4 block channels
- PWM sequence set for 4 switch blocks
- Standalone Mode configuration parameters
- ELINS device ID selected mode
- IO type of TXD
- Six GPIOs configuration parameters
- Free customer data

The system configuration parameters are loaded from the MTP map only when the corresponding MTP load enable code is matched. The load enable codes should be configured when programing the system configuration parameters. Each of the 4 load enable codes can be set independently and control the loading of its corresponding address range. If the load enable code is correct, the system configuration parameters in MTP will replace the default value and the corresponding **MTP_STS.MTP_LOADx** is set to 1.

MTP Load Enable Code		Address Range Start	Address Range End	Bytes Count
MTP_LOAD0	16'h8855	0x0F	0x0F	1
MTP_LOAD1	16'h26AA	0x10	0x65	86
MTP_LOAD2	16'h4C5A	0x70	0x79	10
MTP_LOAD3	16'h34A5	0x80	0x86	7

If the load enable code is incorrect or the MTP has not been programmed yet, the system configuration parameters in MTP will not be loaded. All the configuration fields will keep its default value.

The device provides a safety mechanism when internal MTP fault occurs. When a MTP ECC error happened at address 0x0F in MTP, the device will go into Safe Mode automatically, all PWM width is defined by register **DEFWIDTHx** in MTP, which is same as the Limp-home Mode. The Safe Mode status can be inquired by register **PWM.SAFE_MODE**.

To reprogram MTP storage, please contact indiemicro local support for further detail.

5.17.1 MTP Address Map

ADDR（DEC）	ADDR（HEX）	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	00	MTP LOAD0							
1	01								

ADDR（DEC）	ADDR（HEX）	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
2	02	MTP LOAD1							
3	03								
4	04	MTP LOAD2							
5	05								
6	06	MTP LOAD3							
7	07								
8	08	reserved (56 bits)							
...									
14	0E								
15	0F	reserved	elins speed			pwm_freq_sel			
16	10	reserved				k0_cur0[11:8]			
17	11	k0_cur0[7:0]							
18	12	reserved			k1_cur0[12:8]				
19	13	k1_cur0[7:0]							
20	14	reserved			k2_cur0[12:8]				
21	15	k2_cur0[7:0]							
22	16	reserved			k3_cur0[12:8]				
23	17	k3_cur0[7:0]							
24	18	reserved				k0_cur1[11:8]			
25	19	k0_cur1[7:0]							
26	1A	reserved			k1_cur1[12:8]				
27	1B	k1_cur1[7:0]							
28	1C	reserved			k2_cur1[12:8]				
29	1D	k2_cur1[7:0]							
30	1E	reserved			k3_cur1[12:8]				
31	1F	k3_cur1[7:0]							
32	20	reserved				k0_cur2[11:8]			
33	21	k0_cur2[7:0]							
34	22	reserved			k1_cur2[12:8]				
35	23	k1_cur2[7:0]							
36	24	reserved			k2_cur2[12:8]				
37	25	k2_cur2[7:0]							
38	26	reserved			k3_cur2[12:8]				
39	27	k3_cur2[7:0]							
40	28	reserved				k0_cur3[11:8]			
41	29	k0_cur3[7:0]							
42	2A	reserved			k1_cur3[12:8]				
43	2B	k1_cur3[7:0]							
44	2C	reserved			k2_cur3[12:8]				
45	2D	k2_cur3[7:0]							
46	2E	reserved			k3_cur3[12:8]				
47	2F	k3_cur3[7:0]							
48	30	reserved				k0_cur4[11:8]			
49	31	k0_cur4[7:0]							

ADDR（DEC）	ADDR（HEX）	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
50	32	reserved			k1_cur4[12:8]				
51	33	k1_cur4[7:0]							
52	34	reserved			k2_cur4[12:8]				
53	35	k2_cur4[7:0]							
54	36	reserved			k3_cur4[12:8]				
55	37	k3_cur4[7:0]							
56	38	reserved				k0_cur5[11:8]			
57	39	k0_cur5[7:0]							
58	3A	reserved			k1_cur5[12:8]				
59	3B	k1_cur5[7:0]							
60	3C	reserved			k2_cur5[12:8]				
61	3D	k2_cur5[7:0]							
62	3E	reserved			k3_cur5[12:8]				
63	3F	k3_cur5[7:0]							
64	40	reserved				k0_cur6[11:8]			
65	41	k0_cur6[7:0]							
66	42	reserved			k1_cur6[12:8]				
67	43	k1_cur6[7:0]							
68	44	reserved			k2_cur6[12:8]				
69	45	k2_cur6[7:0]							
70	46	reserved			k3_cur6[12:8]				
71	47	k3_cur6[7:0]							
72	48	reserved				k0_cur7[11:8]			
73	49	k0_cur7[7:0]							
74	4A	reserved			k1_cur7[12:8]				
75	4B	k1_cur7[7:0]							
76	4C	reserved			k2_cur7[12:8]				
77	4D	k2_cur7[7:0]							
78	4E	reserved			k3_cur7[12:8]				
79	4F	k3_cur7[7:0]							
80	50	reserved			cali_bri0				
81	51	reserved			cali_bri1				
82	52	reserved			cali_bri2				
83	53	reserved			cali_bri3				
84	54	reserved			cali_bri4				
85	55	reserved			cali_bri5				
86	56	reserved			cali_bri6				
87	57	reserved			cali_bri7				
88	58	reserved			cali_bri8				
89	59	reserved			cali_bri9				
90	5A	reserved			cali_bri10				
91	5B	reserved			cali_bri11				
92	5C	defwidth1				defwidth0			
93	5D	defwidth3				defwidth2			

ADDR（DEC）	ADDR（HEX）	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
94	5E	defwidth5				defwidth4			
95	5F	defwidth7				defwidth6			
96	60	defwidth9				defwidth8			
97	61	defwidth11				defwidth10			
98	62	reserved	sel_ssc_step			ssc_en	ts_cfg		
99	63	ov_b4cfg		ov_b3cfg		ov_b2cfg		ov_b1cfg	
100	64	sr_b4cfg		sr_b3cfg		sr_b2cfg		sr_b1cfg	
101	65	sel_pwm_sw3		sel_pwm_sw2		sel_pwm_sw1		sel_pwm_sw0	
102	66	reserved (80bits)							
...									
111	6F								
112	70	sel_sam_norm	sam_cfg_width			polar_lhm_ctrl	on2off	trg_mode_fal	trg_mode_wfl
113	71	polar_sig_fal	polar_sig_wfl	sam_delay					
114	72	sam_hold							
115	73	sam_on							
116	74	sam_off							
117	75	reserved		num_flash					
118	76	reserved		wfl_dbnc_thres_p[5:0]					
119	77	reserved		wfl_dbnc_thres_n[5:0]					
120	78	reserved		fal_dbnc_thres_p[5:0]					
121	79	reserved		fal_dbnc_thres_n[5:0]					
122	7A	reserved (48 bits)							
...									
127	7F								
128	80	reserved		addr_mode	gp0_pd	gp0_pu	gp0_pdrv1	gp0_pdrv0	gp0_sl
129	81	reserved			gp1_pd	gp1_pu	gp1_pdrv1	gp1_pdrv0	gp1_sl
130	82	reserved			gp2_pd	gp2_pu	gp2_pdrv1	gp2_pdrv0	gp2_sl
131	83	reserved			gp3_pd	gp3_pu	gp3_pdrv1	gp3_pdrv0	gp3_sl
132	84	reserved			gp4_pd	gp4_pu	gp4_pdrv1	gp4_pdrv0	gp4_sl
133	85	reserved		io_type	gp5_pd	gp5_pu	gp5_pdrv1	gp5_pdrv0	gp5_sl
134	86	reserved			gp6_pd	gp6_pu	gp6_pdrv1	gp6_pdrv0	gp6_sl
135	87	reserved (968 bits)							
...									
255	FF								

5.17.2 MTP Field Description

Field name	Width	Default value	Field description
pwm_freq_sel	4	0x4	Select pwm frequency which is used for the waveform generator after power up. The value also can be set by register after MTP load done. 0x0: PWM frequency: 2.44KHz 0x1: PWM frequency: 1.22KHz 0x2: PWM frequency: 814Hz 0x3: PWM frequency: 610Hz 0x4: PWM frequency: 488Hz 0x5: PWM frequency: 407Hz 0x6: PWM frequency: 349Hz 0x7: PWM frequency: 304Hz 0x8: PWM frequency: 271Hz 0x9: PWM frequency: 244Hz 0xa: PWM frequency: 222Hz
elins speed	3	0x0	Select the baud rate of ELINS. The value also can be set by register after MTP load done. 0x0: elins baud 1Mbps 0x1: elins baud 500Kbps 0x2: elins baud 250Kbps 0x3: elins baud 125Kbps 0x4: elins baud 62.5Kbps 0x5: elins baud 31.25Kbps 0x6: elins baud 31.25Kbps 0x7: elins baud 31.25Kbps
k0_curx(x=0~7)	12	0x0	Set dimming curve coefficient k0. Supports a maximum of eight curve coefficients
k1_curx(x=0~7)	13	0x0	Set dimming curve coefficient k1. Supports a maximum of eight curve coefficients
k2_curx(x=0~7)	13	0x0	Set dimming curve coefficient k2. Supports a maximum of eight curve coefficients
k3_curx(x=0~7)	13	0x0	Set dimming curve coefficient k3. Supports a maximum of eight curve coefficients
cali_brix(x=0~11)	5	0x0	Set 12 LED brightness calibration factors, the brightness reduction can be from 0%(5'h0) to 24.22%(5'h1F).

Field name	Width	Default value	Field description
defwidthx(x=0~11)	4	0x0	Set 12 default pwm widths used in limp home mode. 0x0: Default pwm width in lhm mode: 0 0x1: Default pwm width in lhm mode: 273 0x2: Default pwm width in lhm mode: 546 0x3: Default pwm width in lhm mode: 819 0x4: Default pwm width in lhm mode: 1092 0x5: Default pwm width in lhm mode: 1365 0x6: Default pwm width in lhm mode: 1638 0x7: Default pwm width in lhm mode: 1911 0x8: Default pwm width in lhm mode: 2184 0x9: Default pwm width in lhm mode: 2457 0xa: Default pwm width in lhm mode: 2730 0xb: Default pwm width in lhm mode: 3003 0xc: Default pwm width in lhm mode: 3276 0xd: Default pwm width in lhm mode: 3549 0xe: Default pwm width in lhm mode: 3822 0xf: Default pwm width in lhm mode: 4095
ts_cfg	3	0x0	Choose the OT level from 90~160 degree. 0x0: 160 degree 0x1: 150 degree 0x2: 140 degree 0x3: 130 degree 0x4: 120 degree 0x5: 110 degree 0x6: 100 degree 0x7: 90 degree
ssc_en	1	0x1	SSC Enable.
sel_ssc_step	3	0x6	Set step period used in SSC, in units of 5.5Mhz clock period. 0x0: SSC step period: 2, 42.97kHz 0x1: SSC step period: 3, 28.65kHz 0x2: SSC step period: 4, 21.48kHz 0x3: SSC step period: 5, 17.19kHz 0x4: SSC step period: 6, 14.32kHz 0x5: SSC step period: 7, 12.28kHz 0x6: SSC step period: 8, 10.74kHz 0x7: SSC step period: 9, 9.55kHz
ov_bxcfg(x=1~4)	2	0x1	Set LED OV threshold for LED1~3/LED4~6/LED7~9/LED10~12. 0x0: OV threshold: 6V 0x1: OV threshold: 12V 0x2: OV threshold: 18V 0x3: OV threshold: 21V

Field name	Width	Default value	Field description
sr_bxcfg(x=1~4)	2	0x2	Set LED slew rate threshold for LED1~3/LED4~6/LED7~9/LED10~12. 0x0: slow: 14us 0x1: medium: 4us 0x2: fast: 2us 0x3: fastest: 1us
sel_pwm_sw0 sel_pwm_sw1 sel_pwm_sw2 sel_pwm_sw3	2	0x0 0x1 0x2 0x3	Set pwm sequence of switch block0/1/2/3. 0x0: Select pwm block0 0x1: Select pwm block1 0x2: Select pwm block2 0x3: Select pwm block3
trg_mode_wfl	1	0x0	Waterfall light control mode select: level or edge. Rising edge of signal from gpio trigs a fade scenario. When in level control mode, all LEDs turn off immediately once trg_mode_wfl becomes zero. When in trig control mode, the time of all LEDs ON is set by reg command.
trg_mode_fal	1	0x0	Flashlight control mode select: level or edge. Rising edge of signal from gpio trigs a fade scenario. When in level control mode, all LEDs turn off immediately once trg_mode_fal becomes zero. When in trig control mode, the number of flashlight is set by reg command.
on2off	1	0x0	Set waterfall light play methods. 1'b1: ON->OFF; 1'b0: OFF->ON.
polar_lhm_ctrl	1	0x0	Set the activity polarity of LHM_CTRL from GPIO, 1'b0: active polarity is high 1'b1: active polarity is low.
sam_cfg_width	3	0x0	Set pwm width in standalone mode. 0x0: standalone width: 4095 0x1: standalone width: 511 0x2: standalone width: 1023 0x3: standalone width: 1535 0x4: standalone width: 2047 0x5: standalone width: 2559 0x6: standalone width: 3071 0x7: standalone width: 3583
sel_sam_norm	1	0x0	Select standalone or normal mode. 1'b1: standalone mode 1'b0: normal mode.
sam_delay	6	0x1F	Set standalone Waterfall mode LED delay time. Range from 1ms to 64ms, resolution is 1ms.
polar_sig_wfl	1	0x0	Set the activity polarity of SIG_WFL from GPIO, 1'b0: active polarity is high 1'b1: active polarity is low.
polar_sig_fal	1	0x0	Set the activity polarity of SIG_FAL from GPIO, 1'b0: active polarity is high 1'b1: active polarity is low.
sam_hold	8	0x3F	Set standalone Waterfall mode LED all ON time. Range from 4ms to 1024ms, resolution is 4ms.
sam_on	8	0x3F	Set standalone flashlight mode LED ON time. Range from 4ms to 1024ms, resolution is 4ms.

Field name	Width	Default value	Field description
sam_off	8	0x3F	Set standalone flashlight mode LED OFF time. Range from 4ms to 1024ms, resolution is 4ms.
num_flash	6	0x7	Set standalone flashlight times.
wfl_dbnc_thres_p	6	0x5	Waterfall light control signal debounce threshold from 0 to 1. The deglitch width to detect 1 is from 1 to 64ms.
wfl_dbnc_thres_n	6	0x5	Waterfall light control signal debounce threshold from 1 to 0. The deglitch width to detect 0 is from 1 to 64ms.
fal_dbnc_thres_p	6	0x5	Flashlight control signal debounce threshold from 0 to 1. The deglitch width to detect 1 is from 1 to 64ms.
fal_dbnc_thres_n	6	0x5	Flashlight control signal debounce threshold from 1 to 0. The deglitch width to detect 0 is from 1 to 64ms.
gpx_sl(x=0~6)	1	0x0	GPIO Fast/Slow slew rate select. 1'b0: Fast. 1'b1: Slow
gpx_pdrv0(x=0~6) gpx_pdrv1(x=0~6)	1 1	0x0	GPIO output drive strength selector. {gpx_pdrv1, gpx_pdrv0} Output drive strength 2'b00 4mA 2'b01 8mA 2'b10 12mA 2'b11 16mA
gpx_pu(x=0~6) gpx_pd(x=0~6)	1 1	0x0	GPIO pull-up/pull-down enable. {gpx_pu, gpx_pd} Resistive pulling 2'b00 normal CMOS 2'b01 Pull down 2'b10 Pull up 2'b11 normal CMOS
addr_mode	1	0x0	Select address mode. 1'b0: ADC sample addr0 to decode 5bits address; 1'b1: addr0 is LSB of 3bits address.
io_type	1	0x0	GPIO5 output io type select. 1'b1: pushpull, 1'b0:opendrain.

5.18 ELINS Interface

The ELINS is a slave interface and its data format is based on UART which is a Universal Asynchronous Receiver and Transmitter. The interface works in half duplex mode and the maximum baud rate supported is 1Mbps. The pairs of TXs and RXs pins are internally connected and either pin can be used to connect the iND83080 device to the communication network. This method is convenient for complex PCB layout and wire routing. The interface provides a programmable debouncing filter to filter out glitch of RX data. The RX from 0 to 1 and 1 to 0 debouncing thresholds can be configurated separately. The MCU acts as a communication master, which can write and read the registers by ELINS private protocol to access address space of the iND83080.

If the iND83080 devices and the host are in different boards, a CAN physical layer should be used between different boards. It is helpful to protect from shorts to battery or ground on the cables, and provide better EMI performance. Otherwise, the TX and RX pins should be connected directly, also an external pull-up resistor is needed.

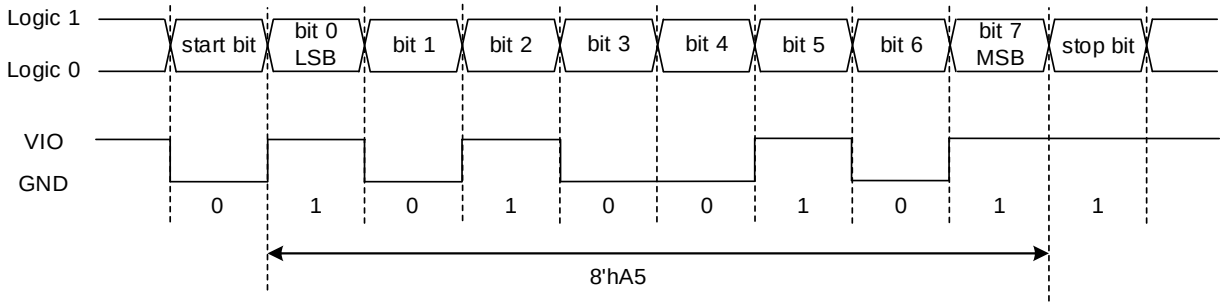
The ELINS supports clock frequency calibration with sync field. All iND83080 devices are synchronized in every ELINS communication frame to ensure a good synchronization and a robust communication. The system clock accuracy would be less than 0.25% after calibration.

The default baud rate of ELINS is stored in MTP, during power on sequence, the default configuration is automatically loaded to register. The baud rate setting will not reset after ELINS reset using register **REQ_ELINS_RSTN**.

- Half-duplex communication (UART compatible)
- One master (MCU)/multi slave(iND83080) architecture
- CAN physical layer
- MCU vs iND83080: CAN PHY with immunity to EMI
- iND83080 vs iND83080: 5V I/O
- Baud rate(bps): 1M/500k/250k/125k/62.5k/31.25k
- Transaction frames: Broadcast Write, Single Device Write, Single Device Read
- Data integrity fully protected by CRC16
- 2 Bits parity checksum for CMD field
- Support clock frequency calibration with sync field
- Clock accuracy after calibration (refer to MCU): ±0.25%

5.18.1 ELINS Byte Format

Each byte field in ELINS, except the break field, is transmitted as the byte field shown in Figure. It operates with one start bit, eight data bits, one stop bit, and no parity (8N1). The LSB of the data is sent first and the MSB last. The start bit is encoded as a bit with value zero (dominant) and the stop bit is encoded as a bit with value one (recessive). The waveform below illustrates a data byte of 8'hA5.



The ELINS baud rate is based on the system clock and can be configurated to the required baud rate(1Mbps/500kbps/250kbps/125kbps/62.5kbps/31.25kbps) with register **ELINS.PRESCL**. The default baud rate is 1Mbps. During power on configuration, the value would be loaded from MTP. The host device could change baud rate through writing this register by broadcast write command. Single write command can't access this register.

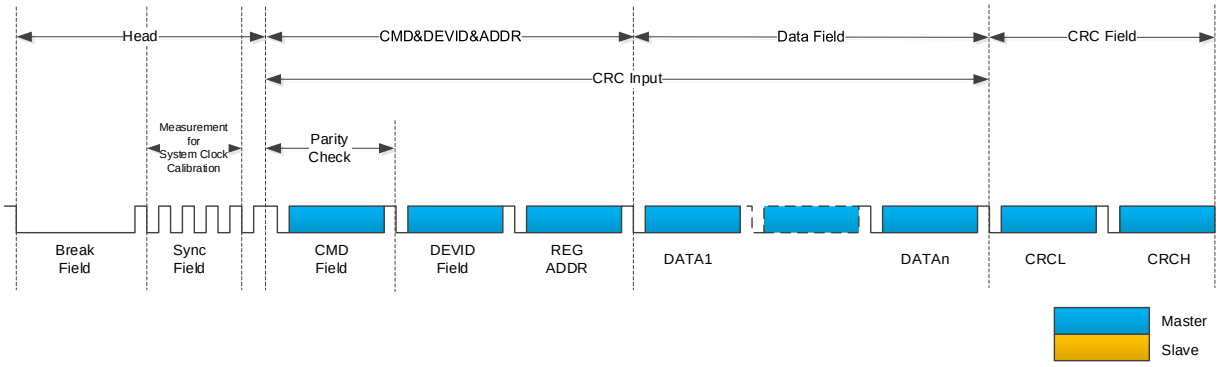
5.18.2 ELINS Communications Protocol

The ELINS interface is as a slave and the MCU controls to initial a communication transaction or not. There are three types of command frames: Broadcast Write, Single Device Write and Single Device Read. Broadcast Write communication has no response frame. Single Device Write communication would have a response frame when **ELINS.ACKENA** in register **ELINS.CTRL** is set to "1".

5.18.2.1 Broadcast Write

Master Command: Break Field + Sync Field + CMD Field + DEVID Field + REG ADDR + N Data Byte(s) + CRC16(2Bytes).

The command frame broadcasts all devices on the communication network and has no response frame.



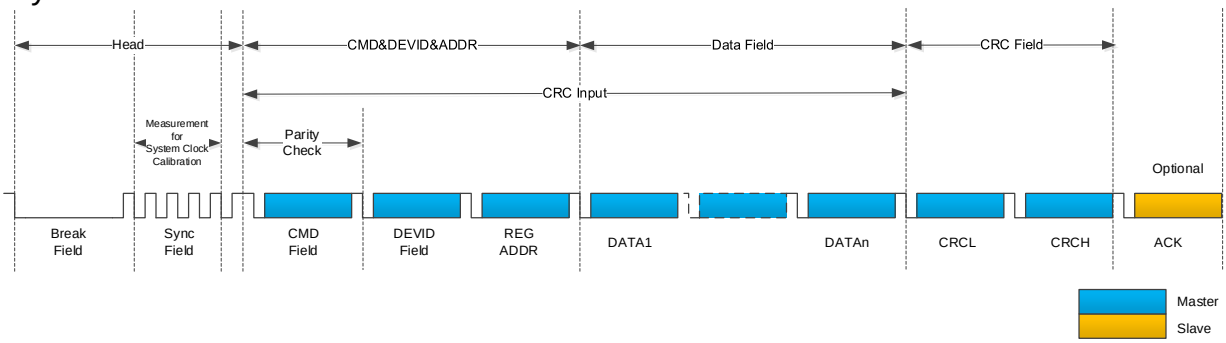
Broadcast Write Diagram

5.18.2.2 Single Device Write

Master Command: Break Field + Sync Field + CMD Field + DEVID Field + REG ADDR + N Data Byte(s) + CRC16(2Bytes).

Slave Response: ACK(Optional).

When ACKENA is set to high and a successful single device write is done (no CRC checksum error and no parity errors), the addressed device transmits an acknowledge back to the MCU. The "ACK" is a single byte which value is equal to {3'b011, DEVID[4:0]}. The register **ELINS.ACKENA** can only be set by a broadcast write.

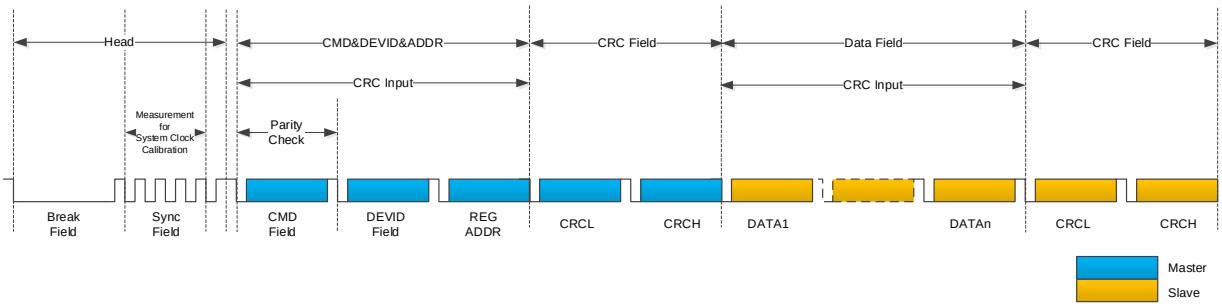


Single Device Write Diagram

5.18.2.3 Single Device Read

Master Command: Break Field + Sync Field + CMD Field + DEVID Field + REG ADDR + CRC16(2Bytes).

Slave Response: N Data Byte(s)+CRC16(2Bytes).



Single Device Read Diagram

5.18.3 ELINS Field Format

The ELINS frames include the following byte fields:

- Break Field
- Sync Field
- CMD Field
- DEVID Field
- The Start Register Address Field (REGADDR)
- Cyclic Redundancy Check Field (CRC)
- N Data Field(s) (N=1,2,3,4,12,16,25 or 32)
- ACK Field

5.18.3.1 Break Field

Break Field is used to signal the beginning of a new frame. It is always generated by the master and it should be at least 9.5 nominal bit times of dominant value, followed by a break delimiter. The break delimiter shall be at least one nominal bit time long.

5.18.3.2 Sync Field

Sync Field is a byte field with the data value 0x55. It is used to calibrate the system clock and makes all devices in a synchronizing system. The ELINS is always able to detect the Break/Sync Field sequence.

5.18.3.3 CMD Field

CMD Field consists of Parity Field(bit7~bit6), DATA_LENGTH Field(bit5~bit3) and CMD_CODE Field(bit2~bit0). A detailed description is shown in the table below.

CMD Field							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
P1	P0	DATA_LENGTH[2:0]			CMD_CODE[2:0]		
P0=CMD[0]+CMD[1]+CMD[2]+CMD[4]							
P1=~(CMD[1]+CMD[3]+CMD[4]+CMD[5])							

DATA_LENGTH[2:0]			Data Bytes
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	12
1	0	1	16
1	1	0	25
1	1	1	32

CMD_CODE[2:0]	Command

0	0	0	Invalid
0	0	1	Invalid
0	1	0	Single Device Write
0	1	1	Single Device Read
1	0	0	Broadcast Write
1	0	1	Invalid
1	1	0	Invalid
1	1	1	Invalid

5.18.4 DEVID and REGADDR Field

DEVID Field							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DEVID[4:0]					REGADDR[10:8]		
REGADDR Field							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
REGADDR[7:0]							

The DEVID bits represent 5 bits device ID, that means up to 32 iND83080 devices can be supported in the one master and multi slave communication network. A broadcast write doesn't care the device ID and can access the address space of all devices.
The REGADDR bits are an eleven-bit start register address and can access 2048 address spaces. The start address is a base address, from which up to 32 successive register locations can be written or read by the master. The register address will wrap back to address 0x000 and continue when a multi-byte communication address increases beyond the address 0x7FF.

5.18.4.1 CRC Field

CRC Field consists of CRCL (CRC low-byte) and CRCH (CRC high-byte) bytes. CRC-16-IBM is used to calculate CRC data on incoming frame data except for data in break and sync field. A CHK flag would be set when a CRC error occurs on an incoming read or write command. The addressed device is also needed to calculate CRC data during the read response, then the master can check the integrity of the read data.

5.18.4.2 Data Field

The number of data bytes to be transferred is decided by DATA_LENGTH, which is located in CMD Field.

5.18.4.3 ACK Field

If the **ACKENA** bit is "1", the addressed device needs to send back an ACK byte following a successful single device write. The ACK byte includes "011" at high three bits and device ID at low five bits. So that the master can get which device to acknowledge.

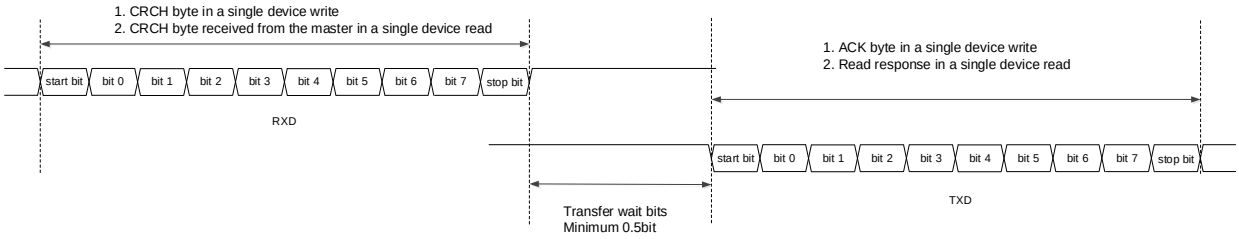
ACK Field							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	1	1	DEVID[4:0]				

5.18.5 ELINS Minimum Transfer Wait Bit

Minimum transfer wait time in unit of bit period should be set in a single device write with an acknowledge byte or in a single device read. The wait time would be at least 0.5 bit length and is

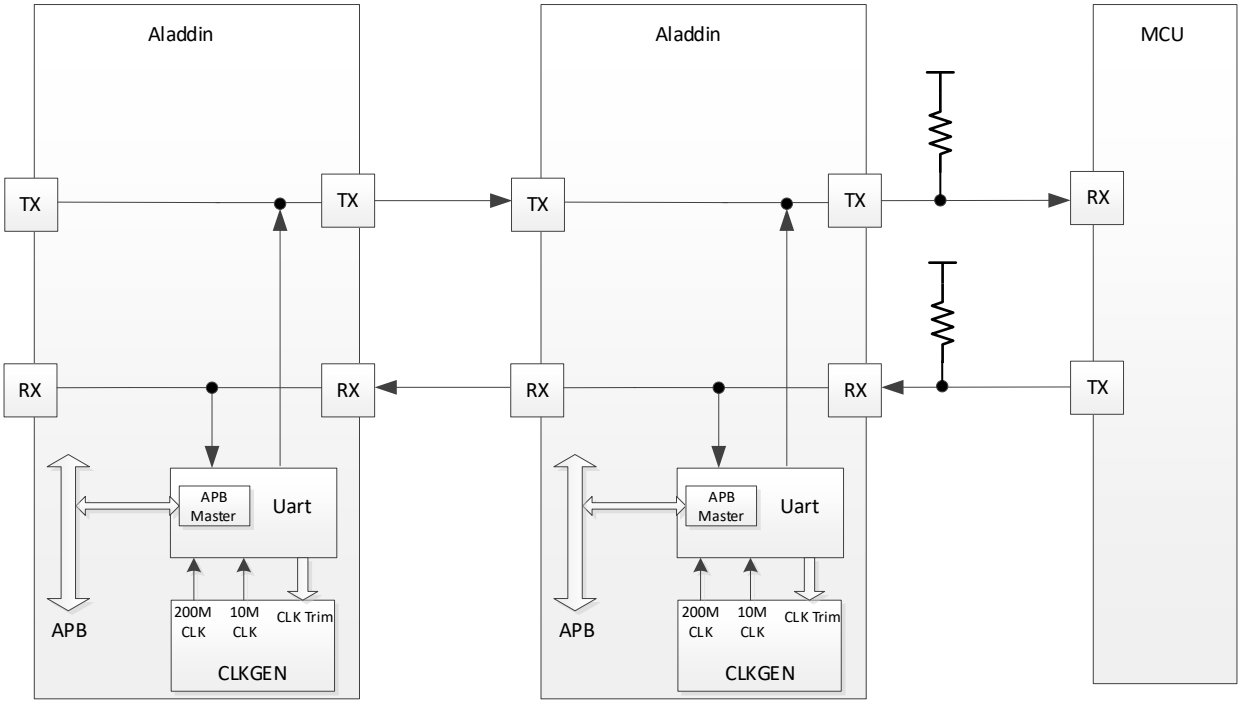
determined by the bigger one between (**TWC_MIN**+0.5) bit length and the time for preparing read data (a write acknowledge data byte or a read response data bytes). Minimum transfer wait time is required in the following cases:

1. Between a single device write command and a write acknowledge (**ACKENA** = 1)
2. Between a single device read command and a read response

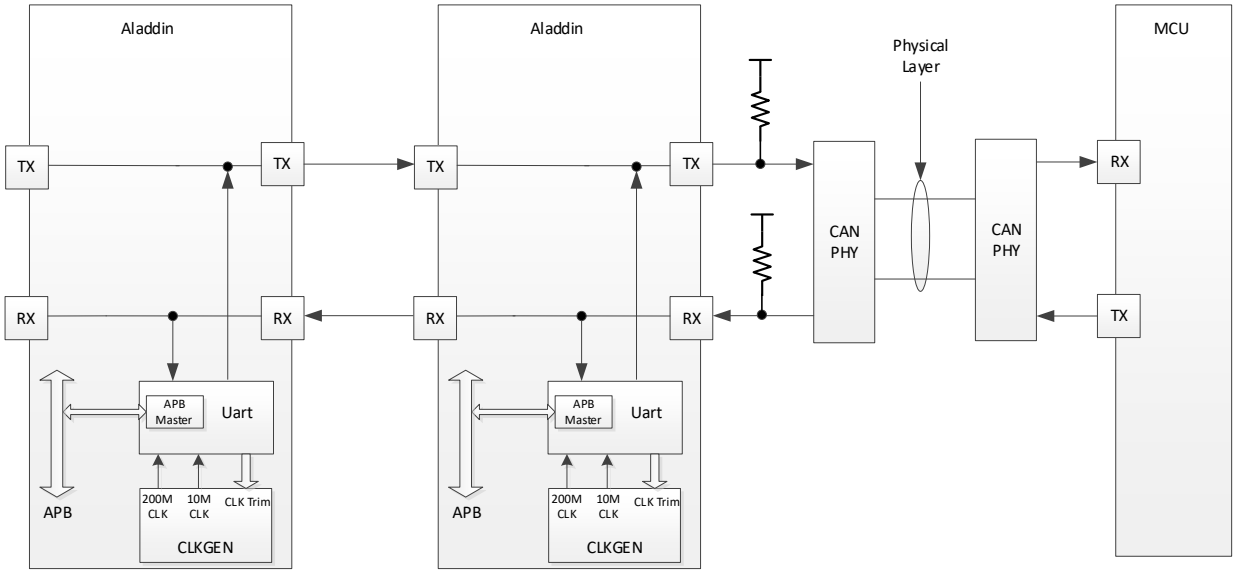


5.18.6 ELINS Physical Layer

If the iND83080 devices and the MCU are on the same board, the TX and RX pins should be connected directly, as well as a pull-up resistor(open-drain) and a connection topology between TX and RX pins. The TX pin should be driven by an open-drain(default) or push-pull buffer, which is controlled by register **IOTYPE** in MTP and the configuration value can be autoload after power-up. It would be set to open-drain structure according to one master and multi slave system structure. The inactive state of the TX and RX pin is high while the device is powering on.



If the iND83080 devices and the MCU are in different boards, a CAN physical layer should be used between the TX and RX pins. It is helpful to protect from shorts to battery or ground on the cables, and more immune to EMI. The ELINS interface needs to provide a half-duplex protocol to compatible with CAN transceivers.


Aladdin
Aladdin
Physical Layer
MCU
TX
TX
TX
TX
RX
RX
RX
RX
CAN PHY
CAN PHY
RX
TX
APB Master
Uart
APB
200M CLK
10M CLK
CLK Trim
CLKGEN
APB Master
Uart
APB
200M CLK
10M CLK
CLK Trim
CLKGEN

6 Register Map

Aladdin MCM Map		
Address	**Peripheral Name**	**Description**
0x0 - 0x3F	CRGA	Clock & Reset Generator
0x40 - 0x7F	PMUA	Power Management Unit
0x80 - 0xFF	WDT_BARIUM	Watchdog Timer Registers
0x100 - 0x27F	PWM	Pulse Width Modulation waveform generator.
0x280 - 0x2BF	SAR_CTRL	SAR ADC Interface registers
0x300 - 0x3FF	SYSCTRLA	System configuration
0x400 - 0x4FF	ELINS	ELIN slave interface registers
0x540 - 0x55F	MTP	MTP configuration registers

Note:

- Only the registers listed below are allowed to write, writing operation on other registers could cause unexpected behavior
- Return value of write-only(wo) registers is undefined
- Return value of some readable registers is various according to different hardware versions, which are marked with N/A in Reset value column, e.g. ASICNAME, REV

6.1 Clock & Reset Generator

CRGA		
Address	**Register Name**	**Description**
0x4	CRGARSTN	System reset control

6.1.1 CRGARSTN

0x4 — **CRGARSTN** — ^

System reset control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F9	F8	F7	F6	-	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F9	POR_FLAG	Power on reset flag. Set by the hardware during power-on reset	1	ro	0x1
F8	BOR_1V5_FLAG	BOR 1v5 flag. Set by the hardware when a brownout of the 1.5V supply is detected.	1	ro	0x1
F7	POR_FLAG_CLR	POR flag clear. Set 1 to clear the POR flag	1	wo	N/A
F6	BOR_1V5_FLAG_CLR	BOR 1v5 clear. Set 1 to clear the 1.5V brownout detected flag	1	wo	N/A
F4	REQ_SOFT_RSTN	Soft reset request. Set 1 to trig a soft reset of chip	1	wo	N/A
F3	REQ_MTP_RSTN	MTP soft reset request. Set 1 to trig a soft reset of MTP module.	1	wo	N/A
F2	REQ_PWM_RSTN	PWM soft reset request. Set 1 to trig a soft reset of PWM module.	1	wo	N/A
F1	REQ_ELINS_RSTN	ELINS soft reset request. Set 1 to trig a soft reset of ELINS module.	1	wo	N/A
F0	REQ_ADC_RSTN	ADC soft reset request. Set 1 to trig a soft reset of ADC module.	1	wo	N/A

6.2 Power Management Unit

PMUA		
Address	**Register Name**	**Description**
0x40	CP_CFG_STS	Charge pump configuration & state

6.2.1 CP_CFG_STS

0x40 CP_CFG_STS ^

Charge pump configuration & state.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F16	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F16	CLR_VCPP_ERROR	Write 1 to CLR_VCPP_ERROR to clear all FLAG_VCPP_ERROR.	1	wo	0x0
F0	FLAG_VCPP_ERROR	FLAG_VCPP_ERROR[b]=1(b=0~3): a vcpp error in the corresponding block has happened, FLAG_VCPP_ERROR[b]=0(b=0~3): a vcpp error in the corresponding block didn't happen.	4	ro	0x0

6.3 Watchdog Timer Registers

WDT_BARIUM		
Address	**Register Name**	**Description**
0x80	CTRL	Control
0x88	CNTVAL	Counter value

6.3.1 CTRL

0x80 CTRL ^

Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F24	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F24	RUNNING	WDT running status. A flag indicates when the watchdog timer is running. 0x0: Watchdog timer is stopped and cleared 0x1: Watchdog timer is running	1	ro	N/A
F8	UPDATE	UPDATE. Set to update Watchdog Configurations.	1	dual	0x0
F0	TIMEOUT_SEL	Timeout select. Defines the watchdog timeout period (the time between a clear operation and the next timeout). 0x0: 2^10 * 8us = 8.192ms 0x1: 2^11 * 8us = 16.384ms 0x2: 2^12 * 8us = 32.768ms 0x3: 2^13 * 8us = 65.536ms 0x4: 2^14 * 8us = 131.072ms 0x5: 2^15 * 8us = 262.144ms 0x6: 2^16 * 8us = 524.288ms 0x7: 2^17 * 8us = 1048.576ms	3	rw	0x7

6.3.2 CNTVAL

0x88 CNTVAL ^

Counter value.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	CNTVAL	Counter value. The instantaneous value of watchdog timeout counter	32	ro	0x0

6.4 Pulse Width Modulation waveform generator.

PWM		
Address	**Register Name**	**Description**
0x100	PWM_CTRL	PWM control register
0x110	ENA_REQ_STS	PWM enable request & status

0x114	PWMWIDTH0	Set widths of PWM pulse0 and pulse1
0x118	PWMWIDTH1	Set widths of PWM pulse2 and pulse3
0x11C	PWMWIDTH2	Set widths of PWM pulse4 and pulse5
0x120	PWMWIDTH3	Set widths of PWM pulse6 and pulse7
0x124	PWMWIDTH4	Set widths of PWM pulse8 and pulse9
0x128	PWMWIDTH5	Set widths of PWM pulse10 and pulse11
0x12C	UPDATE	UPDATE
0x16C	SMARTBUSY	SMART_BUSY
0x170	SRTCH00	Smart mode channel0 configuration0
0x174	SRTCH01	Smart mode channel0 configuration1
0x178	SRTCH10	Smart mode channel1 configuration0
0x17C	SRTCH11	Smart mode channel1 configuration1
0x180	SRTCH20	Smart mode channel2 configuration0
0x184	SRTCH21	Smart mode channel2 configuration1
0x188	SRTCH30	Smart mode channel3 configuration0
0x18C	SRTCH31	Smart mode channel3 configuration1
0x190	SRTCH40	Smart mode channel4 configuration0
0x194	SRTCH41	Smart mode channel4 configuration1
0x198	SRTCH50	Smart mode channel5 configuration0
0x19C	SRTCH51	Smart mode channel5 configuration1
0x1A0	SRTCH60	Smart mode channel6 configuration0
0x1A4	SRTCH61	Smart mode channel6 configuration1
0x1A8	SRTCH70	Smart mode channel7 configuration0
0x1AC	SRTCH71	Smart mode channel7 configuration1
0x1B0	SRTCH80	Smart mode channel8 configuration0
0x1B4	SRTCH81	Smart mode channel8 configuration1
0x1B8	SRTCH90	Smart mode channel9 configuration0
0x1BC	SRTCH91	Smart mode channel9 configuration1
0x1C0	SRTCHA0	Smart mode channel10 configuration0
0x1C4	SRTCHA1	Smart mode channel10 configuration1
0x1C8	SRTCHB0	Smart mode channel11 configuration0
0x1CC	SRTCHB1	Smart mode channel11 configuration1

6.4.1 PWM_CTRL

0x100 PWM_CTRL ^

PWM control register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																-	-	-	-	-	-	-	-	F4				-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F16	CODE_MANU_UPDATE	Set 16 bits code to set update method. When set to 16'hE9A2, the pwm parameters are updated by write 1 to register(update), otherwise the parameters are auto updated when period pulse.	16	rw	0x0
F4	PWM_FREQ_SEL	Select pwm frequency which is used for the waveform generator.During power on configuration, the default value will be loaded from MTP. It can only be reset by hardware. 0x0: PWM frequency: 2.44KHz 0x1: PWM frequency: 1.22KHz 0x2: PWM frequency: 814Hz 0x3: PWM frequency: 610Hz 0x4: PWM frequency: 488Hz 0x5: PWM frequency: 407Hz 0x6: PWM frequency: 349Hz 0x7: PWM frequency: 304Hz 0x8: PWM frequency: 271Hz 0x9: PWM frequency: 244Hz 0xa: PWM frequency: 222Hz 0xb: PWM frequency: 203Hz 0xc: PWM frequency: 188Hz 0xd: PWM frequency: 174Hz 0xe: PWM frequency: 163Hz 0xf: PWM frequency: 153Hz	4	rw	0x4
F0	FPHASE_SEL	Set different phase shift mode. 0x0: Phase shift by 64 0x1: Phase shift by 128 0x2: Phase shift by 256 0x3: Phase shift by 341	2	rw	0x2

6.4.2 ENA_REQ_STS

0x110 ENA_REQ_STS ^

PWM enable request & status.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F16												F15	F14	F13	F12	F0											

#	Field Name	Field Description	Width	Access	Reset
F16	ENA_STS	Status of enable in the waveform generator.	12	ro	0x0
F15	SAFE_MODE	Safe mode status, when the chip is in safe mode, all pwm widths are set to defwidth, which is same as in limphome mode.	1	ro	0x0
F14	FORCE_INACTIVE	Set to force PWM signals return to initial value immediately.	1	rw	0x0
F13	CLR_REQ_ALL	Write 1 to clear all ENA_REQ bits; Write 0 has no effects.	1	wo	0x0
F12	ENA_REQ_ALL	Write 1 to enable all ENA_REQ bits; Write 0 has no effects.	1	wo	0x0
F0	ENA_REQ	Set to enable the waveform generator.	12	rw	0x0

6.4.3 PWMWIDTH0

0x114 **PWMWIDTH0** ^

Set widths of PWM pulse0 and pulse1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F16												-	-	-	-	F0											

#	Field Name	Field Description	Width	Access	Reset
F16	WIDTH1	Pulse1 width. Set the pulse width of PWM1 waveform.	12	rw	0x0
F0	WIDTH0	Pulse0 width. Set the pulse width of PWM0 waveform.	12	rw	0x0

6.4.4 PWMWIDTH1

0x118 **PWMWIDTH1** ^

Set widths of PWM pulse2 and pulse3.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F16												-	-	-	-	F0											

#	Field Name	Field Description	Width	Access	Reset
F16	WIDTH3	Pulse3 width. Set the pulse width of PWM3 waveform.	12	rw	0x0
F0	WIDTH2	Pulse2 width. Set the pulse width of PWM2 waveform.	12	rw	0x0

6.4.5 PWMWIDTH2

0x11C **PWMWIDTH2** ^

Set widths of PWM pulse4 and pulse5.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F16												-	-	-	-	F0											

#	Field Name	Field Description	Width	Access	Reset
F16	WIDTH5	Pulse5 width. Set the pulse width of PWM5 waveform.	12	rw	0x0
F0	WIDTH4	Pulse4 width. Set the pulse width of PWM4 waveform.	12	rw	0x0

6.4.6 PWMWIDTH3

0x120 **PWMWIDTH3** ^

Set widths of PWM pulse6 and pulse7.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F16												-	-	-	-	F0											

#	Field Name	Field Description	Width	Access	Reset
F16	WIDTH7	Pulse7 width. Set the pulse width of PWM7 waveform.	12	rw	0x0
F0	WIDTH6	Pulse6 width. Set the pulse width of PWM6 waveform.	12	rw	0x0

6.4.7 PWMWIDTH4

0x124 **PWMWIDTH4** ^

Set widths of PWM pulse8 and pulse9.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F16												-	-	-	-	F0											

#	Field Name	Field Description	Width	Access	Reset

F16	WIDTH9	Pulse9 width. Set the pulse width of PWM9 waveform.	12	rw	0x0
F0	WIDTH8	Pulse8 width. Set the pulse width of PWM8 waveform.	12	rw	0x0

6.4.8 PWMWIDTH5

0x128 **PWMWIDTH5** ^

Set widths of PWM pulse10 and pulse11.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F16												-	-	-	-	F0											

#	Field Name	Field Description	Width	Access	Reset
F16	WIDTH11	Pulse11 width. Set the pulse width of PWM11 waveform.	12	rw	0x0
F0	WIDTH10	Pulse10 width. Set the pulse width of PWM10 waveform.	12	rw	0x0

6.4.9 UPDATE

0x12C **UPDATE** ^

UPDATE.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	UPDATE	Set to trigger consumption of new PULSE parameters (pulse width & phase). The flag is automatically cleared by the hardware when the settings are consumed, so reading a high value indicates that an update is still pending.	1	dual	N/A

6.4.10 SMARTBUSY

0x16C **SMARTBUSY** ^

SMART_BUSY.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0											

#	Field Name	Field Description	Width	Access	Reset
F0	SMART_BUSY	When smart_busy[11:0] become high, the corresponding pwm sequrnce in smart mode is running.	12	ro	0x0

6.4.11 SRTCH00

0x170 **SRTCH00** ^

Smart mode channel0 configuration0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F28			-	F24			-	-	-	-	F16				-	-	F8						-	F4			-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F28	HOLD_TIMEUNIT_SEL0	Set the hold timeunit. 0x0: hold timeunit: 1ms 0x1: hold timeunit: 2ms 0x2: hold timeunit: 4ms 0x3: hold timeunit: 6ms 0x4: hold timeunit: 10ms 0x5: hold timeunit: 16ms 0x6: hold timeunit: 32ms 0x7: hold timeunit: 64ms	3	rw	0x2
F24	DELAY_TIMEUNIT_SEL0	Set the delay timeunit. 0x0: delay timeunit: 1ms 0x1: delay timeunit: 2ms 0x2: delay timeunit: 4ms 0x3: delay timeunit: 6ms 0x4: delay timeunit: 10ms 0x5: delay timeunit: 16ms 0x6: delay timeunit: 32ms 0x7: delay timeunit: 64ms	3	rw	0x2
F16	NUM_DECIM0	Set the decimation factor in units of sample points. 0: original PWM sample data; others: the decimation factor is NUM_DECIM0[3:0].	4	rw	0x0
F8	STEP_PRD0	Set the step period in units of 1ms. Range from 1ms to 64ms.	6	rw	0x0
F4	CUR_SEL0	Dimming curve coefficient selection. Eight dimming curve coefficients can be selected with the three bits.	3	rw	0x0
F2	NXT0	Start a new smart sequence after the current smart sequence is done.	1	dual	0x0
F1	NOW0	Start a new smart sequence immediately during the current smart sequence. When the bit is set during the current smart sequence, the new smart parameters to the specific channel changes immediately then the new smart sequence starts.	1	dual	0x0

F0	PLAY0	set 1 to trig a sequence play. autoclear after the sequence play is done.	1	dual	0x0

6.4.12 SRTCH01

0x174 **SRTCH01** ^

Smart mode channel0 configuration1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	HOLD0	Set the hold time after a smart sequence. Set hold time, hold[7:0]*hold timeunit.	8	rw	0x0
F16	DELAY0	Set the delay time before a smart sequence. Set delay time, delay[7:0]*delay timeunit.	8	rw	0x0
F8	STOP_STEP0	Set the stop step. The stop step can be set from 0 to 255.	8	rw	0xFF
F0	START_STEP0	Set the start step. The start step can be set from 0 to 255.	8	rw	0x0

6.4.13 SRTCH10

0x178 **SRTCH10** ^

Smart mode channel1 configuration0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F28			-	F24			-	-	-	-	F16				-	-	F8						-	F4			-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F28	HOLD_TIMEUNIT_SEL1	Set the hold timeunit. 0x0: hold timeunit: 1ms 0x1: hold timeunit: 2ms 0x2: hold timeunit: 4ms 0x3: hold timeunit: 6ms 0x4: hold timeunit: 10ms 0x5: hold timeunit: 16ms 0x6: hold timeunit: 32ms 0x7: hold timeunit: 64ms	3	rw	0x2
F24	DELAY_TIMEUNIT_SEL1	Set the delay timeunit. 0x0: delay timeunit: 1ms 0x1: delay timeunit: 2ms 0x2: delay timeunit: 4ms 0x3: delay timeunit: 6ms 0x4: delay timeunit: 10ms 0x5: delay timeunit: 16ms 0x6: delay timeunit: 32ms 0x7: delay timeunit: 64ms	3	rw	0x2
F16	NUM_DECIM1	Set the decimation factor in units of sample points. 0: original PWM sample data; others: the decimation factor is NUM_DECIM1[3:0].	4	rw	0x0
F8	STEP_PRD1	Set the step period in units of 1ms. Range from 1ms to 64ms.	6	rw	0x0
F4	CUR_SEL1	Dimming curve coefficient selection. Eight dimming curve coefficients can be selected with the three bits.	3	rw	0x0
F2	NXT1	Start a new smart sequence after the current smart sequence is done.	1	dual	0x0
F1	NOW1	Start a new smart sequence immediately during the current smart sequence. When the bit is set during the current smart sequence, the new smart parameters to the specific channel changes immediately then the new smart sequence starts.	1	dual	0x0
F0	PLAY1	set 1 to trig a sequence play. autoclear after the sequence play is done.	1	dual	0x0

6.4.14 SRTCH11

0x17C **SRTCH11** ^

Smart mode channel1 configuration1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	HOLD1	Set the hold time after a smart sequence. Set hold time, hold[7:0]*hold timeunit.	8	rw	0x0
F16	DELAY1	Set the delay time before a smart sequence. Set delay time, delay[7:0]*delay timeunit.	8	rw	0x0
F8	STOP_STEP1	Set the stop step. The stop step can be set from 0 to 255.	8	rw	0xFF
F0	START_STEP1	Set the start step. The start step can be set from 0 to 255.	8	rw	0x0

6.4.15 SRTCH20

0x180 **SRTCH20** ^

Smart mode channel2 configuration0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F28			-	F24			-	-	-	-	F16				-	-	F8						-	F4			-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F28	HOLD_TIMEUNIT_SEL2	Set the hold timeunit. 0x0: hold timeunit: 1ms 0x1: hold timeunit: 2ms 0x2: hold timeunit: 4ms 0x3: hold timeunit: 6ms 0x4: hold timeunit: 10ms 0x5: hold timeunit: 16ms 0x6: hold timeunit: 32ms 0x7: hold timeunit: 64ms	3	rw	0x2
F24	DELAY_TIMEUNIT_SEL2	Set the delay timeunit. 0x0: delay timeunit: 1ms 0x1: delay timeunit: 2ms 0x2: delay timeunit: 4ms 0x3: delay timeunit: 6ms 0x4: delay timeunit: 10ms 0x5: delay timeunit: 16ms 0x6: delay timeunit: 32ms 0x7: delay timeunit: 64ms	3	rw	0x2
F16	NUM_DECIM2	Set the decimation factor in units of sample points. 0: original PWM sample data; others: the decimation factor is NUM_DECIM2[3:0].	4	rw	0x0
F8	STEP_PRD2	Set the step period in units of 1ms. Range from 1ms to 64ms.	6	rw	0x0
F4	CUR_SEL2	Dimming curve coefficient selection. Eight dimming curve coefficients can be selected with the three bits.	3	rw	0x0
F2	NXT2	Start a new smart sequence after the current smart sequence is done.	1	dual	0x0
F1	NOW2	Start a new smart sequence immediately during the current smart sequence. When the bit is set during the current smart sequence, the new smart parameters to the specific channel changes immediately then the new smart sequence starts.	1	dual	0x0
F0	PLAY2	set 1 to trig a sequence play. autoclear after the sequence play is done.	1	dual	0x0

6.4.16 SRTCH21

0x184 **SRTCH21** ^

Smart mode channel2 configuration1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	HOLD2	Set the hold time after a smart sequence. Set hold time, hold[7:0]*hold timeunit.	8	rw	0x0
F16	DELAY2	Set the delay time before a smart sequence. Set delay time, delay[7:0]*delay timeunit.	8	rw	0x0
F8	STOP_STEP2	Set the stop step. The stop step can be set from 0 to 255.	8	rw	0xFF
F0	START_STEP2	Set the start step. The start step can be set from 0 to 255.	8	rw	0x0

6.4.17 SRTCH30

0x188 **SRTCH30** ^

Smart mode channel3 configuration0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F28			-	F24			-	-	-	-	F16				-	-	F8						-	F4			-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F28	HOLD_TIMEUNIT_SEL3	Set the hold timeunit. 0x0: hold timeunit: 1ms 0x1: hold timeunit: 2ms 0x2: hold timeunit: 4ms 0x3: hold timeunit: 6ms 0x4: hold timeunit: 10ms 0x5: hold timeunit: 16ms 0x6: hold timeunit: 32ms 0x7: hold timeunit: 64ms	3	rw	0x2
F24	DELAY_TIMEUNIT_SEL3	Set the delay timeunit. 0x0: delay timeunit: 1ms 0x1: delay timeunit: 2ms 0x2: delay timeunit: 4ms 0x3: delay timeunit: 6ms 0x4: delay timeunit: 10ms 0x5: delay timeunit: 16ms 0x6: delay timeunit: 32ms 0x7: delay timeunit: 64ms	3	rw	0x2
F16	NUM_DECIM3	Set the decimation factor in units of sample points. 0: original PWM sample data; others: the decimation factor is NUM_DECIM3[3:0].	4	rw	0x0
F8	STEP_PRD3	Set the step period in units of 1ms. Range from 1ms to 64ms.	6	rw	0x0

F4	CUR_SEL3	Dimming curve coefficient selection. Eight dimming curve coefficients can be selected with the three bits.	3	rw	0x0
F2	NXT3	Start a new smart sequence after the current smart sequence is done.	1	dual	0x0
F1	NOW3	Start a new smart sequence immediately during the current smart sequence. When the bit is set during the current smart sequence, the new smart parameters to the specific channel changes immediately then the new smart sequence starts.	1	dual	0x0
F0	PLAY3	set 1 to trig a sequence play. autoclear after the sequence play is done.	1	dual	0x0

6.4.18 SRTCH31

0x18C **SRTCH31** ^

Smart mode channel3 configuration1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	HOLD3	Set the hold time after a smart sequence. Set hold time, hold[7:0]*hold timeunit.	8	rw	0x0
F16	DELAY3	Set the delay time before a smart sequence. Set delay time, delay[7:0]*delay timeunit.	8	rw	0x0
F8	STOP_STEP3	Set the stop step. The stop step can be set from 0 to 255.	8	rw	0xFF
F0	START_STEP3	Set the start step. The start step can be set from 0 to 255.	8	rw	0x0

6.4.19 SRTCH40

0x190 **SRTCH40** ^

Smart mode channel4 configuration0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F28			-	F24			-	-	-	-	F16				-	-	F8						-	F4			-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F28	HOLD_TIMEUNIT_SEL4	Set the hold timeunit. 0x0: hold timeunit: 1ms 0x1: hold timeunit: 2ms 0x2: hold timeunit: 4ms 0x3: hold timeunit: 6ms 0x4: hold timeunit: 10ms 0x5: hold timeunit: 16ms 0x6: hold timeunit: 32ms 0x7: hold timeunit: 64ms	3	rw	0x2
F24	DELAY_TIMEUNIT_SEL4	Set the delay timeunit. 0x0: delay timeunit: 1ms 0x1: delay timeunit: 2ms 0x2: delay timeunit: 4ms 0x3: delay timeunit: 6ms 0x4: delay timeunit: 10ms 0x5: delay timeunit: 16ms 0x6: delay timeunit: 32ms 0x7: delay timeunit: 64ms	3	rw	0x2
F16	NUM_DECIM4	Set the decimation factor in units of sample points. 0: original PWM sample data; others: the decimation factor is NUM_DECIM4[3:0].	4	rw	0x0
F8	STEP_PRD4	Set the step period in units of 1ms. Range from 1ms to 64ms.	6	rw	0x0
F4	CUR_SEL4	Dimming curve coefficient selection. Eight dimming curve coefficients can be selected with the three bits.	3	rw	0x0
F2	NXT4	Start a new smart sequence after the current smart sequence is done.	1	dual	0x0
F1	NOW4	Start a new smart sequence immediately during the current smart sequence. When the bit is set during the current smart sequence, the new smart parameters to the specific channel changes immediately then the new smart sequence starts.	1	dual	0x0
F0	PLAY4	set 1 to trig a sequence play. autoclear after the sequence play is done.	1	dual	0x0

6.4.20 SRTCH41

0x194 **SRTCH41** ^

Smart mode channel4 configuration1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	HOLD4	Set the hold time after a smart sequence. Set hold time, hold[7:0]*hold timeunit.	8	rw	0x0
F16	DELAY4	Set the delay time before a smart sequence. Set delay time, delay[7:0]*delay timeunit.	8	rw	0x0
F8	STOP_STEP4	Set the stop step. The stop step can be set from 0 to 255.	8	rw	0xFF
F0	START_STEP4	Set the start step. The start step can be set from 0 to 255.	8	rw	0x0

6.4.21 SRTCH50

0x198 **SRTCH50** ^

Smart mode channel5 configuration0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F28			-	F24			-	-	-	-	F16				-	-	F8						-	F4			-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F28	HOLD_TIMEUNIT_SEL5	Set the hold timeunit. 0x0: hold timeunit: 1ms 0x1: hold timeunit: 2ms 0x2: hold timeunit: 4ms 0x3: hold timeunit: 6ms 0x4: hold timeunit: 10ms 0x5: hold timeunit: 16ms 0x6: hold timeunit: 32ms 0x7: hold timeunit: 64ms	3	rw	0x2
F24	DELAY_TIMEUNIT_SEL5	Set the delay timeunit. 0x0: delay timeunit: 1ms 0x1: delay timeunit: 2ms 0x2: delay timeunit: 4ms 0x3: delay timeunit: 6ms 0x4: delay timeunit: 10ms 0x5: delay timeunit: 16ms 0x6: delay timeunit: 32ms 0x7: delay timeunit: 64ms	3	rw	0x2
F16	NUM_DECIM5	Set the decimation factor in units of sample points. 0: original PWM sample data; others: the decimation factor is NUM_DECIM2[3:0].	4	rw	0x0
F8	STEP_PRD5	Set the step period in units of 1ms. Range from 1ms to 64ms.	6	rw	0x0
F4	CUR_SEL5	Dimming curve coefficient selection. Eight dimming curve coefficients can be selected with the three bits.	3	rw	0x0
F2	NXT5	Start a new smart sequence after the current smart sequence is done.	1	dual	0x0
F1	NOW5	Start a new smart sequence immediately during the current smart sequence. When the bit is set during the current smart sequence, the new smart parameters to the specific channel changes immediately then the new smart sequence starts.	1	dual	0x0
F0	PLAY5	set 1 to trig a sequence play. autoclear after the sequence play is done.	1	dual	0x0

6.4.22 SRTCH51

0x19C **SRTCH51** ^

Smart mode channel5 configuration1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	HOLD5	Set the hold time after a smart sequence. Set hold time, hold[7:0]*hold timeunit.	8	rw	0x0
F16	DELAY5	Set the delay time before a smart sequence. Set delay time, delay[7:0]*delay timeunit.	8	rw	0x0
F8	STOP_STEP5	Set the stop step. The stop step can be set from 0 to 255.	8	rw	0xFF
F0	START_STEP5	Set the start step. The start step can be set from 0 to 255.	8	rw	0x0

6.4.23 SRTCH60

0x1A0 **SRTCH60** ^

Smart mode channel6 configuration0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F28			-	F24			-	-	-	-	F16				-	-	F8						-	F4			-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F28	HOLD_TIMEUNIT_SEL6	Set the hold timeunit. 0x0: hold timeunit: 1ms 0x1: hold timeunit: 2ms 0x2: hold timeunit: 4ms 0x3: hold timeunit: 6ms 0x4: hold timeunit: 10ms 0x5: hold timeunit: 16ms 0x6: hold timeunit: 32ms 0x7: hold timeunit: 64ms	3	rw	0x2
F24	DELAY_TIMEUNIT_SEL6	Set the delay timeunit. 0x0: delay timeunit: 1ms 0x1: delay timeunit: 2ms 0x2: delay timeunit: 4ms 0x3: delay timeunit: 6ms 0x4: delay timeunit: 10ms 0x5: delay timeunit: 16ms	3	rw	0x2

		0x6: delay timeunit: 32ms 0x7: delay timeunit: 64ms			
F16	NUM_DECIM6	Set the decimation factor in units of sample points. 0: original PWM sample data; others: the decimation factor is NUM_DECIM6[3:0].	4	rw	0x0
F8	STEP_PRD6	Set the step period in units of 1ms. Range from 1ms to 64ms.	6	rw	0x0
F4	CUR_SEL6	Dimming curve coefficient selection. Eight dimming curve coefficients can be selected with the three bits.	3	rw	0x0
F2	NXT6	Start a new smart sequence after the current smart sequence is done.	1	dual	0x0
F1	NOW6	Start a new smart sequence immediately during the current smart sequence. When the bit is set during the current smart sequence, the new smart parameters to the specific channel changes immediately then the new smart sequence starts.	1	dual	0x0
F0	PLAY6	set 1 to trig a sequence play. autoclear after the sequence play is done.	1	dual	0x0

6.4.24 SRTCH61

0x1A4 **SRTCH61** ^

Smart mode channel6 configuration1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	HOLD6	Set the hold time after a smart sequence. Set hold time, hold[7:0]*hold timeunit.	8	rw	0x0
F16	DELAY6	Set the delay time before a smart sequence. Set delay time, delay[7:0]*delay timeunit.	8	rw	0x0
F8	STOP_STEP6	Set the stop step. The stop step can be set from 0 to 255.	8	rw	0xFF
F0	START_STEP6	Set the start step. The start step can be set from 0 to 255.	8	rw	0x0

6.4.25 SRTCH70

0x1A8 **SRTCH70** ^

Smart mode channel7 configuration0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F28			-	F24			-	-	-	-	F16				-	-	F8						-	F4			-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F28	HOLD_TIMEUNIT_SEL7	Set the hold timeunit. 0x0: hold timeunit: 1ms 0x1: hold timeunit: 2ms 0x2: hold timeunit: 4ms 0x3: hold timeunit: 6ms 0x4: hold timeunit: 10ms 0x5: hold timeunit: 16ms 0x6: hold timeunit: 32ms 0x7: hold timeunit: 64ms	3	rw	0x2
F24	DELAY_TIMEUNIT_SEL7	Set the delay timeunit. 0x0: delay timeunit: 1ms 0x1: delay timeunit: 2ms 0x2: delay timeunit: 4ms 0x3: delay timeunit: 6ms 0x4: delay timeunit: 10ms 0x5: delay timeunit: 16ms 0x6: delay timeunit: 32ms 0x7: delay timeunit: 64ms	3	rw	0x2
F16	NUM_DECIM7	Set the decimation factor in units of sample points. 0: original PWM sample data; others: the decimation factor is NUM_DECIM7[3:0].	4	rw	0x0
F8	STEP_PRD7	Set the step period in units of 1ms. Range from 1ms to 64ms.	6	rw	0x0
F4	CUR_SEL7	Dimming curve coefficient selection. Eight dimming curve coefficients can be selected with the three bits.	3	rw	0x0
F2	NXT7	Start a new smart sequence after the current smart sequence is done.	1	dual	0x0
F1	NOW7	Start a new smart sequence immediately during the current smart sequence. When the bit is set during the current smart sequence, the new smart parameters to the specific channel changes immediately then the new smart sequence starts.	1	dual	0x0
F0	PLAY7	set 1 to trig a sequence play. autoclear after the sequence play is done.	1	dual	0x0

6.4.26 SRTCH71

0x1AC **SRTCH71** ^

Smart mode channel7 configuration1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset

F24	HOLD7	Set the hold time after a smart sequence. Set hold time, hold[7:0]*hold timeunit.	8	rw	0x0
F16	DELAY7	Set the delay time before a smart sequence. Set delay time, delay[7:0]*delay timeunit.	8	rw	0x0
F8	STOP_STEP7	Set the stop step. The stop step can be set from 0 to 255.	8	rw	0xFF
F0	START_STEP7	Set the start step. The start step can be set from 0 to 255.	8	rw	0x0

6.4.27 SRTCH80

0x1B0 **SRTCH80** ^

Smart mode channel8 configuration0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F28			-	F24			-	-	-	-	F16				-	-	F8						-	F4			-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F28	HOLD_TIMEUNIT_SEL8	Set the hold timeunit. 0x0: hold timeunit: 1ms 0x1: hold timeunit: 2ms 0x2: hold timeunit: 4ms 0x3: hold timeunit: 6ms 0x4: hold timeunit: 10ms 0x5: hold timeunit: 16ms 0x6: hold timeunit: 32ms 0x7: hold timeunit: 64ms	3	rw	0x2
F24	DELAY_TIMEUNIT_SEL8	Set the delay timeunit. 0x0: delay timeunit: 1ms 0x1: delay timeunit: 2ms 0x2: delay timeunit: 4ms 0x3: delay timeunit: 6ms 0x4: delay timeunit: 10ms 0x5: delay timeunit: 16ms 0x6: delay timeunit: 32ms 0x7: delay timeunit: 64ms	3	rw	0x2
F16	NUM_DECIM8	Set the decimation factor in units of sample points. 0: original PWM sample data; others: the decimation factor is NUM_DECIM8[3:0].	4	rw	0x0
F8	STEP_PRD8	Set the step period in units of 1ms. Range from 1ms to 64ms.	6	rw	0x0
F4	CUR_SEL8	Dimming curve coefficient selection. Eight dimming curve coefficients can be selected with the three bits.	3	rw	0x0
F2	NXT8	Start a new smart sequence after the current smart sequence is done.	1	dual	0x0
F1	NOW8	Start a new smart sequence immediately during the current smart sequence. When the bit is set during the current smart sequence, the new smart parameters to the specific channel changes immediately then the new smart sequence starts.	1	dual	0x0
F0	PLAY8	set 1 to trig a sequence play. autoclear after the sequence play is done.	1	dual	0x0

6.4.28 SRTCH81

0x1B4 **SRTCH81** ^

Smart mode channel8 configuration1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	HOLD8	Set the hold time after a smart sequence. Set hold time, hold[7:0]*hold timeunit.	8	rw	0x0
F16	DELAY8	Set the delay time before a smart sequence. Set delay time, delay[7:0]*delay timeunit.	8	rw	0x0
F8	STOP_STEP8	Set the stop step. The stop step can be set from 0 to 255.	8	rw	0xFF
F0	START_STEP8	Set the start step. The start step can be set from 0 to 255.	8	rw	0x0

6.4.29 SRTCH90

0x1B8 **SRTCH90** ^

Smart mode channel9 configuration0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F28			-	F24			-	-	-	-	F16				-	-	F8						-	F4			-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F28	HOLD_TIMEUNIT_SEL9	Set the hold timeunit. 0x0: hold timeunit: 1ms 0x1: hold timeunit: 2ms 0x2: hold timeunit: 4ms 0x3: hold timeunit: 6ms 0x4: hold timeunit: 10ms 0x5: hold timeunit: 16ms 0x6: hold timeunit: 32ms 0x7: hold timeunit: 64ms	3	rw	0x2

F24	DELAY_TIMEUNIT_SEL9	Set the delay timeunit. 0x0: delay timeunit: 1ms 0x1: delay timeunit: 2ms 0x2: delay timeunit: 4ms 0x3: delay timeunit: 6ms 0x4: delay timeunit: 10ms 0x5: delay timeunit: 16ms 0x6: delay timeunit: 32ms 0x7: delay timeunit: 64ms	3	rw	0x2
F16	NUM_DECIM9	Set the decimation factor in units of sample points. 0: original PWM sample data; others: the decimation factor is NUM_DECIM9[3:0].	4	rw	0x0
F8	STEP_PRD9	Set the step period in units of 1ms. Range from 1ms to 64ms.	6	rw	0x0
F4	CUR_SEL9	Dimming curve coefficient selection. Eight dimming curve coefficients can be selected with the three bits.	3	rw	0x0
F2	NXT9	Start a new smart sequence after the current smart sequence is done.	1	dual	0x0
F1	NOW9	Start a new smart sequence immediately during the current smart sequence. When the bit is set during the current smart sequence, the new smart parameters to the specific channel changes immediately then the new smart sequence starts.	1	dual	0x0
F0	PLAY9	set 1 to trig a sequence play. autoclear after the sequence play is done.	1	dual	0x0

6.4.30 SRTCH91

0x1BC **SRTCH91** ^

Smart mode channel9 configuration1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	HOLD9	Set the hold time after a smart sequence. Set hold time, hold[7:0]*hold timeunit.	8	rw	0x0
F16	DELAY9	Set the delay time before a smart sequence. Set delay time, delay[7:0]*delay timeunit.	8	rw	0x0
F8	STOP_STEP9	Set the stop step. The stop step can be set from 0 to 255.	8	rw	0xFF
F0	START_STEP9	Set the start step. The start step can be set from 0 to 255.	8	rw	0x0

6.4.31 SRTCHA0

0x1C0 **SRTCHA0** ^

Smart mode channel10 configuration0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F28			-	F24			-	-	-	-	F16				-	-	F8						-	F4			-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F28	HOLD_TIMEUNIT_SEL10	Set the hold timeunit. 0x0: hold timeunit: 1ms 0x1: hold timeunit: 2ms 0x2: hold timeunit: 4ms 0x3: hold timeunit: 6ms 0x4: hold timeunit: 10ms 0x5: hold timeunit: 16ms 0x6: hold timeunit: 32ms 0x7: hold timeunit: 64ms	3	rw	0x2
F24	DELAY_TIMEUNIT_SEL10	Set the delay timeunit. 0x0: delay timeunit: 1ms 0x1: delay timeunit: 2ms 0x2: delay timeunit: 4ms 0x3: delay timeunit: 6ms 0x4: delay timeunit: 10ms 0x5: delay timeunit: 16ms 0x6: delay timeunit: 32ms 0x7: delay timeunit: 64ms	3	rw	0x2
F16	NUM_DECIM10	Set the decimation factor in units of sample points. 0: original PWM sample data; others: the decimation factor is NUM_DECIM10[3:0].	4	rw	0x0
F8	STEP_PRD10	Set the step period in units of 1ms. Range from 1ms to 64ms.	6	rw	0x0
F4	CUR_SEL10	Dimming curve coefficient selection. Eight dimming curve coefficients can be selected with the three bits.	3	rw	0x0
F2	NXT10	Start a new smart sequence after the current smart sequence is done.	1	dual	0x0
F1	NOW10	Start a new smart sequence immediately during the current smart sequence. When the bit is set during the current smart sequence, the new smart parameters to the specific channel changes immediately then the new smart sequence starts.	1	dual	0x0
F0	PLAY10	set 1 to trig a sequence play. autoclear after the sequence play is done.	1	dual	0x0

6.4.32 SRTCHA1

0x1C4 **SRTCHA1** ^

Smart mode channel10 configuration1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	HOLD10	Set the hold time after a smart sequence. Set hold time, hold[7:0]*hold timeunit.	8	rw	0x0
F16	DELAY10	Set the delay time before a smart sequence. Set delay time, delay[7:0]*delay timeunit.	8	rw	0x0
F8	STOP_STEP10	Set the stop step. The stop step can be set from 0 to 255.	8	rw	0xFF
F0	START_STEP10	Set the start step. The start step can be set from 0 to 255.	8	rw	0x0

6.4.33 SRTCHB0

0x1C8 **SRTCHB0** ^

Smart mode channel11 configuration0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F28			-	F24			-	-	-	-	F16				-	-	F8						-	F4			-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F28	HOLD_TIMEUNIT_SEL11	Set the hold timeunit. 0x0: delay timeunit: 1ms 0x1: delay timeunit: 2ms 0x2: delay timeunit: 4ms 0x3: delay timeunit: 6ms 0x4: delay timeunit: 10ms 0x5: delay timeunit: 16ms 0x6: delay timeunit: 32ms 0x7: delay timeunit: 64ms	3	rw	0x2
F24	DELAY_TIMEUNIT_SEL11	Set the delay timeunit. 0x0: delay timeunit: 1ms 0x1: delay timeunit: 2ms 0x2: delay timeunit: 4ms 0x3: delay timeunit: 6ms 0x4: delay timeunit: 10ms 0x5: delay timeunit: 16ms 0x6: delay timeunit: 32ms 0x7: delay timeunit: 64ms	3	rw	0x2
F16	NUM_DECIM11	Set the decimation factor in units of sample points. 0: original PWM sample data; others: the decimation factor is NUM_DECIM11[3:0].	4	rw	0x0
F8	STEP_PRD11	Set the step period in units of 1ms. Range from 1ms to 64ms.	6	rw	0x0
F4	CUR_SEL11	Dimming curve coefficient selection. Eight dimming curve coefficients can be selected with the three bits.	3	rw	0x0
F2	NXT11	Start a new smart sequence after the current smart sequence is done.	1	dual	0x0
F1	NOW11	Start a new smart sequence immediately during the current smart sequence. When the bit is set during the current smart sequence, the new smart parameters to the specific channel changes immediately then the new smart sequence starts.	1	dual	0x0
F0	PLAY11	set 1 to trig a sequence play. autoclear after the sequence play is done.	1	dual	0x0

6.4.34 SRTCHB1

0x1CC **SRTCHB1** ^

Smart mode channel11 configuration1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	HOLD11	Set the hold time after a smart sequence. Set hold time, hold[7:0]*hold timeunit.	8	rw	0x0
F16	DELAY11	Set the delay time before a smart sequence. Set delay time, delay[7:0]*delay timeunit.	8	rw	0x0
F8	STOP_STEP11	Set the stop step. The stop step can be set from 0 to 255.	8	rw	0xFF
F0	START_STEP11	Set the start step. The start step can be set from 0 to 255.	8	rw	0x0

6.5 SAR ADC Interface registers

SAR_CTRL

Address	Register Name	Description

0x280	SAR_CTRL	SAR ADC Control
0x284	SAR_CFG	SAR Configuration Register
0x288	SAR_CHAN_CONF	SAR Channel Configuration
0x28C	ADC_DATA0	ADC_DATA0,
0x290	ADC_DATA1	ADC_DATA1,
0x294	ADC_DATA2	ADC_DATA2,
0x298	ADC_DATA3	ADC_DATA3,
0x29C	ADC_DATA4	ADC_DATA4,
0x2A0	SAR_INT	SAR Interrupts

6.5.1 SAR_CTRL

0x280 SAR_CTRL ^

SAR ADC Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F16	-	F14	F12		F10		F9	F8	-	-	-	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F16	SAR_BUSY	SAR ADC busy. When SAR ADC is running, the flag is set	1	ro	0x0
F14	EN_AVER	Enable sample data average.	1	rw	0x0
F12	AVER_SEL	Select average numbers of adc sample data. 0x0: Average numbers of adc sample data: 4 0x1: Average numbers of adc sample data: 8 0x2: Average numbers of adc sample data: 16 0x3: Average numbers of adc sample data: 32	2	rw	0x0
F10	SEL_SAR_CLK	Select the SAR ADC reference clock. 0x0: ADC reference clock: 1Mhz 0x1: ADC reference clock: 2Mhz 0x2: ADC reference clock: 3.3Mhz 0x3: ADC reference clock: 1Mhz	2	rw	0x0
F9	AUTO_TRG_EN	Automatic sampling conversion Enable. When auto_trg_en is high, the ADC would take a sample every 128ms.	1	rw	0x0
F8	CONT	Continuous Conversion Enable. If this bit has been set before an ADC conversion sequence trigged by CONVERT bit, the sequence will be treated as a sequential conversion, rather than a single conversion, only value when auto_trg_en is disable.	1	rw	0x0
F4	DIG_RESET	SAR Digital Part Reset. Resets SAR digital parts.	1	wo	N/A
F3	CONVERT	ADC START Register. Set 1 to start a new adc conversion. NOTE: THAT BIT SHOULD NOT BE SET UNTIL ALL OTHER CONFIG BITS BE SETTED Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F2	SAR_AFE_EN	ADC AFE Enable. adc afe enable. If vinp, vinn and vin vcm all choose external, adc afe should be disabled: adc_adc_en=0, otherwise, adc afe must be enabled: adc_afe_en=1.	1	rw	0x0
F1	SAR_PREAMP_EN	adc pre-amp enable. 0:disable, 1:enable	1	rw	0x0
F0	SAR_ENA_REQ	SAR ADC Enable. Set to enable the SAR analog & digital part	1	rw	0x0

6.5.2 SAR_CFG

0x284 SAR_CFG ^

SAR Configuration Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	F16								F12				F10		-	-	-	-	-	-	F2		F0	

#	Field Name	Field Description	Width	Access	Reset
F16	TRIG_DLY	trigger delay. Set trigger delay time from 1 to 256 sar clock cycles.	8	rw	0x15
F12	SAMPCYC	Sample cycle. Set sampling time from 1 to 16 sar clock cycles. 0x0: 1 Cycle 0x1: 2 Cycle 0x2: 3 Cycle 0xf: 16 Cycle	4	rw	0x7
F10	SEL_OT_DBNC_THRES	Select OT flag debounce threshold. 0x0: 32us 0x1: 64us 0x2: 96us 0x3: 128us	2	rw	0x3
F2	SAR_INPUT_GAIN	choose ADC input gain. When ADDR0 channel is sampling, the sar input gain is force to 31/32. 0x0: 14/32 0x1: 22/32 0x2: 31/32 0x3: 31/32	2	rw	0x0
F0	ADC_VREF_SEL	adc vref select. When ADDR0 channel is sampling, the adc vref value is force to VDD_5V0. 0x0: adc_vref = vbg when sar_ena_req=1	2	rw	0x1

		0x1: adc_vref = 2*vbg when sar_ena_req=1 0x2: adc_vref = VDD_5V0 when sar_ena_req=1 0x3: adc_vref = VDD_5V0 when sar_ena_req=1			

6.5.3 SAR_CHAN_CONF

0x288 **SAR_CHAN_CONF** ^

SAR Channel Configuration.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	F16			-	F12			-	F8			-	F4			-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F16	CH4_SEL	Channel4 Selection. Refer to Channel1 Selects.	3	rw	0x4
F12	CH3_SEL	Channel3 Selection. Refer to Channel1 Selects.	3	rw	0x3
F8	CH2_SEL	Channel2 Selection. Refer to Channel1 Selects.	3	rw	0x2
F4	CH1_SEL	Channel1 Selection. Channel1 Selects. 0x0: REF_GND 0x1: PAD_ADC1 0x2: PAD_ADC2 0x3: ADC_TSP, four temperature sample data are obtained from four switch block 0x4: ADC_TSN, four temperature sample data are obtained from four switch block 0x5: ADDR0 0x6: ADC_REFP 0x7: VDD_V1P5	3	rw	0x1
F0	CHAN_SEQ_NUM	Channel Sequence number. Select the sequence number of channels to be converted. 0x0: CH1 only 0x1: CH1->CH2 0x2: CH1->CH2->CH3 0x3: CH1->CH2->CH3->CH4	2	rw	0x3

6.5.4 ADC_DATA0

0x28C **ADC_DATA0** ^

ADC_DATA0,.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F16												-	-	-	-	F0											

#	Field Name	Field Description	Width	Access	Reset
F16	DATA1	Data1 of ADC conversion	12	ro	0x0
F0	DATA0	Data0 of ADC conversion	12	ro	0x0

6.5.5 ADC_DATA1

0x290 **ADC_DATA1** ^

ADC_DATA1,.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F16												-	-	-	-	F0											

#	Field Name	Field Description	Width	Access	Reset
F16	DATA3	Data3 of ADC conversion	12	ro	0x0
F0	DATA2	Data2 of ADC conversion	12	ro	0x0

6.5.6 ADC_DATA2

0x294 **ADC_DATA2** ^

ADC_DATA2,.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F16												-	-	-	-	F0											

#	Field Name	Field Description	Width	Access	Reset
F16	DATA5	Data5 of ADC conversion	12	ro	0x0
F0	DATA4	Data4 of ADC conversion	12	ro	0x0

6.5.7 ADC_DATA3

0x298 **ADC_DATA3** ^

ADC_DATA3,.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F16												-	-	-	-	F0											

#	Field Name	Field Description	Width	Access	Reset
F16	DATA7	Data7 of ADC conversion	12	ro	0x0
F0	DATA6	Data6 of ADC conversion	12	ro	0x0

6.5.8 ADC_DATA4

0x29C — **ADC_DATA4** ^

ADC_DATA4,.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F16												-	-	-	-	F0											

#	Field Name	Field Description	Width	Access	Reset
F16	DATA9	Data9 of ADC conversion	12	ro	0x0
F0	DATA8	Data8 of ADC conversion	12	ro	0x0

6.5.9 SAR_INT

0x2A0 — **SAR_INT** ^

SAR Interrupts. Contains the enable, status and clear for the SAR interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F25	F24	-	-	-	F20	F19	F18	F17	F16	-	-	-	-	-	-	F9	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F25	INT_OT	Over-temperature Interrupt.	1	ro	0x0
F24	INT_SAR_DONE	SAR Convert Done Interrupt.	1	ro	0x0
F20	STS_OT0	Over-temperature flag of OT channel 0. Set when an Over-temperature happens.	1	ro	0x0
F19	STS_OT1	Over-temperature flag of OT channel 1. Set when an Over-temperature happens.	1	ro	0x0
F18	STS_OT2	Over-temperature flag of OT channel 2. Set when an Over-temperature happens.	1	ro	0x0
F17	STS_OT3	Over-temperature flag of OT channel 3. Set when an Over-temperature happens.	1	ro	0x0
F16	STS_SAR_DONE	SAR Convert Done Status. Set by the SAR when an conversion is done.	1	ro	0x0
F9	INT_OT_CLR	Over-temperature Interrupt Clear.	1	wo	N/A
F8	INT_SAR_DONE_CLR	SAR Convert Done Interrupt Clear.	1	wo	N/A
F1	INT_OT_ENA	Over-temperature Interrupt Enable.	1	rw	0x0
F0	INT_SAR_DONE_ENA	SAR Convert Done Interrupt Enable.	1	rw	0x0

6.6 System configuration

SYSCTRLA

Address	Register Name	Description
0x32C	SYS_STATUS	System status
0x330	SYS_CFG	System parameter configuration
0x334	LHM_DEACTIVE	lhm deactive configuration
0x340	FLAG_OV_SC	LED overvoltage & short-circuit flag
0x344	ASICNAME	ASIC_NAME
0x348	REV	Silicon Revision

6.6.1 SYS_STATUS

0x32C — **SYS_STATUS** ^

System status.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F9	POR_FLAG	Power on reset flag. Set by the hardware during power-on reset	1	ro	N/A
F8	BOR_1V5_FLAG	BOR 1v5 flag. Set by the hardware when a brownout of the 1.5V supply is detected.	1	ro	N/A

F7	WDT_RUNNING	The watchdog timer is running when WDT_RUNNING is high.	1	ro	N/A
F6	PWM_RUNNING	The PWM counter is running when PWM_RUNNING is high.	1	ro	N/A
F5	LHM_MODE	The chip is working in limphome mode when LHM_MODE is high.	1	ro	N/A
F4	MTP_ERROR	A status flag indicates MTP ECC error has occurred.	1	ro	N/A
F3	VCPP_ERROR	A status flag indicates a vcpp error has occurred.	1	ro	N/A
F2	OT	A status flag indicates an over-temperature has occurred.	1	ro	N/A
F1	SC	A status flag indicates a LED short-circuit has occurred.	1	ro	N/A
F0	OV	A status flag indicates a LED overvoltage has occurred.	1	ro	N/A

6.6.2 SYS_CFG

0x330 **SYS_CFG** ^

System parameter configuration.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	F24						-	-	F16						F15	-	-	-	-	-	-	-	-	-	-	F4	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F24	LHM_DBNC_THRES_N	LHM_CTRL debounce threshold from 1 to 0. The deglitch width to detect 0 is from 1 to 64ms.	6	rw	0x7
F16	LHM_DBNC_THRES_P	LHM_CTRL debounce threshold from 0 to 1. The deglitch width to detect 1 is from 1 to 64ms.	6	rw	0x7
F15	EN_TS_CFG	Set temperature sense enable.	1	rw	0x1
F4	UPDATE_SHADOW	Update shadow register.	1	wo	0x0
F0	WORK_MODE	Set the work mode. 0x0: Direct Mode 0x1: Smart Mode	2	rw	0x0

6.6.3 LHM_DEACTIVE

0x334 **LHM_DEACTIVE** ^

lhm deactive configuration.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F16	F0															

#	Field Name	Field Description	Width	Access	Reset
F16	DEACTIVE_LHM	Set 1 to deactive lhm mode when deactive_lhm_code is 0x9116.	1	wo	0x0
F0	DEACTIVE_LHM_CODE	The code used to deactive lhm mode. Before deactive lhm mode, the deactive lhm code must be set to 0x9116.	16	rw	0x0

6.6.4 FLAG_OV_SC

0x340 **FLAG_OV_SC** ^

LED overvoltage & short-circuit flag.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F29		F28	F16												-	-	-	F12	F0											

#	Field Name	Field Description	Width	Access	Reset
F29	SEL_SC_DGH	Set the diglitch time of all short-circuit state signals. 0x0: SC deglitch time: 32 us 0x1: SC deglitch time: 64 us 0x2: SC deglitch time: 128us 0x3: SC deglitch time: 256us	2	rw	0x2
F28	CLR_SC	Write 1 to CLR_SC to clear all FLAG_SC.	1	wo	0x0
F16	FLAG_SC	LED SC flag=1: LED voltage is short; LED SC flag=0: LED voltage is not short.	12	ro	0x0
F12	CLR_OV	Write 1 to CLR_OV to clear all FLAG_OV.	1	wo	0x0
F0	FLAG_OV	LED OV flag=1: LED voltage is over threshold; LED OV flag=0: LED voltage is not over threshold.	12	ro	0x0

6.6.5 ASICNAME

0x344 **ASICNAME** ^

ASIC_NAME.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	ASICNAME	ASIC name. A read from this register will return the ASIC name	32	ro	N/A

6.6.6 REV

0x348 **REV** ^

Silicon Revision.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	REV	Silicon Revision. A read from this register will return the ASCII silicon revision (e.g. ASCII A0 is 0x4130)	16	ro	N/A

6.7 ELIN slave interface registers

ELINS

Address	Register Name	Description
0x404	CTRL	Control Register
0x408	ERROR	Error Register
0x40C	ID	ID Register

6.7.1 CTRL

0x404 **CTRL** ^

Control Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	F24						-	-	F16						-	-	-	-	-	-	-	-	-	F4			F1			F0

#	Field Name	Field Description	Width	Access	Reset
F24	HYST1SEL	RXD 0 to 1 hysteris threshold select. The hysteris threshold = HYST0_SEL * 5ns(Cycle time of one FLL clock).	6	rw	0x1
F16	HYST0SEL	RXD 1 to 0 hysteris threshold select. The hysteris threshold = HYST0_SEL * 5ns(Cycle time of one FLL clock).	6	rw	0x1
F4	TWCMIN	Minimum Transfer Wait Bit Count. Determine the minimum wait bit count between the address field of a read command and the data transfer from the slave. The real transfer wait timing is determined by the bigger one between TWC_MIN*TQ and the time for preparing read data.	3	rw	0x2
F1	PRESCL	Prescaler Register. Prescaler Setting. Determine the baud rate of ELIN. During power on configuration, the default value will be loaded from MTP. Master could change baud-rate through writing this register by broadcast write command. Single write command can not access this register. It can only be reset by hardware. 0x0: elins baud 1Mbps 0x1: elins baud 500Kbps 0x2: elins baud 250Kbps 0x3: elins baud 125Kbps 0x4: elins baud 62.5Kbps 0x5: elins baud 31.25Kbps 0x6: elins baud 31.25Kbps 0x7: elins baud 31.25Kbps	3	rw	0x0
F0	ACKENA	Acknowledge Enable. Set to enable acknowedge to a successful single write command.This register could only be written by broadcast write command.Single write command can not access this register.	1	rw	0x0

6.7.2 ERROR

0x408 **ERROR** ^

Error Register. The errors flags will be cleared automatically once the register is read

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F6	F5	-	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F6	FRAMEERR	Byte Field Framing Error. This bit is set by the ELIN core slave if a transmission is aborted after the beginning of the data field due to a timeout or an incomplete frame	1	ro	0x0
F5	SBITERR	Start Bit Error in Byte field. Start Bit Error in Byte field, i.e., invalid start bit.	1	ro	0x0
F3	PARITY	Parity Error. Identifier parity error	1	ro	0x0
F2	TIMEOUT	Timeout Error. There are several reason that can cause a timeout error: The master detects a timeout error if it is expecting data from the bus but no slave does respond. If the slave responds to late and the frame is not finished within the maximum frame length TFRAME_MAX a timeout error	1	ro	0x0

		will be detected too. The slave detects a timeout error if it is requesting a data acknowledge to the host controller (for selecting receive or transmit, data length and loading data), and the host controller does not set CTRL.DATA_ACK or CTRL.STOP register until the end of the reception of the first byte after the identifier. The slave detects a timeout error if it has transmitted a wakeup signal and it detects no sync field (from the master) within 150 ms. Note: The slave does not perform an exact check of the frame length TFRAME_MAX but a timeout is detected after 200 bit times, if the slave is in receive mode and there are missing data fields or a missing ID field from the master.			
F1	CHK	Checksum Error. Checksum Error	1	ro	0x0
F0	BITERR	Bit Error in Byte field. Bit Error in Byte field, i.e., invalid stop bit.	1	ro	0x0

6.7.3 ID

0x40C **ID** ^

ID Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0					

#	Field Name	Field Description	Width	Access	Reset
F0	ID	ID. ID register, frame identifier	6	rw	0x0

6.8 MTP configuration registers

MTP		
Address	**Register Name**	**Description**
0x540	MTP_CTR0	MTP control register0
0x548	MTP_CTR2	MTP control register2
0x54C	MTP_ADDR	MTP address register
0x554	MTP_RD	MTP read data
0x55C	MTP_STS	MTP status register

To reprogram MTP storage, please contact indiemicro local support for further detail.

6.8.1 MTP_CTR0

0x540 **MTP_CTR0** ^

MTP control register0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	F17	-	-	-	-	-	-	-	-	-	-	-	F0					

#	Field Name	Field Description	Width	Access	Reset
F17	MTP_START	MTP_START. Set 1 to trig a MTP start.	1	wo	0x0
F0	MTP_MODE	MTP_MODE. Set MTP work mode. 0x0: read mode	7	rw	0x0

6.8.2 MTP_CTR2

0x548 **MTP_CTR2** ^

MTP control register2.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F3	F2	-	-

#	Field Name	Field Description	Width	Access	Reset
F3	CLR_ECC_FAIL	CLR_ECC_FAIL. Write 1 to clear flag_ecc_fail; Write 0 has no effects.	1	wo	0x0
F2	CLR_DATA_ERR	CLR_DATA_ERR. Write 1 to clear flag_data_err_1b and flag_data_err_2b; Write 0 has no effects.	1	wo	0x0

6.8.3 MTP_ADDR

0x54C **MTP_ADDR** ^

MTP address register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F8	MTP_NUM_RD	Set MTP consecutive read addresses. The sum of MTP_ADDR and MTP_NUM_RD is from 0 to 255.	8	rw	0xFF
F0	MTP_ADDR	MTP address. Set mtp address, range from 0 to 255.	8	rw	0x0

6.8.4 MTP_RD

0x554 **MTP_RD** ^

MTP read data.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-							F0						

#	Field Name	Field Description	Width	Access	Reset
F0	MTP_DATA_RD	MTP read data.	13	ro	0x0

6.8.5 MTP_STS

0x55C **MTP_STS** ^

MTP status register.

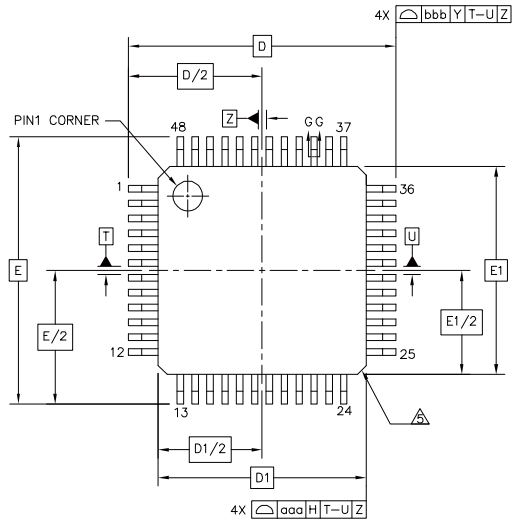
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F11	F10	F8		-	-	-	-	-	-	F1	-

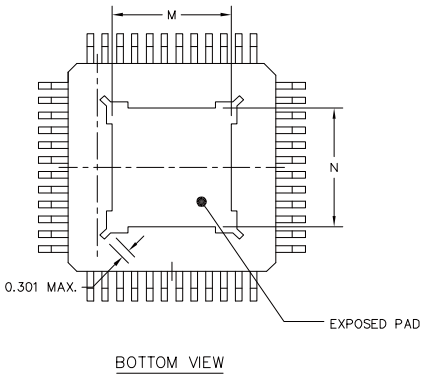
#	Field Name	Field Description	Width	Access	Reset
F11	FLAG_DATA_ERR_2B	The FLAG_DATA_ERR_2B bit indicates more than 2 bits error bits has be detected when MTP read mode.	1	ro	N/A
F10	FLAG_DATA_ERR_1B	The FLAG_DATA_ERR_1B bit indicates 1 bit error bits has be detected when MTP read mode.	1	ro	N/A
F8	MTP_PERR	MTP ERROR. 0x0: no error bits detected. 0x1: 1 bit error detected and corrected. 0x2: more than 2bits error detected, can't be corrected. 0x3: don't care.	2	ro	0x0
F1	MTP_BUSY	When MTP_BUSY becomes 1, MTP is running read/program/ECC test	1	ro	0x0

Note:

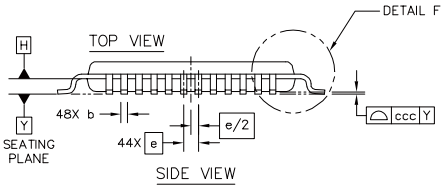
7 Package Information

Package Information of iND83080:

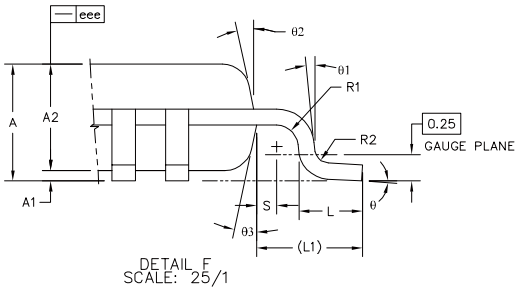




BOTTOM VIEW

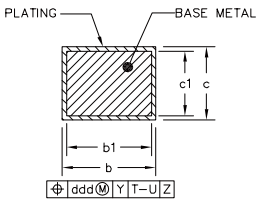


SIDE VIEW



DETAIL F
SCALE: 25/1

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.2
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	0.95	1	1.05
LEAD WIDTH(PLATING)		b	0.17	0.22	0.27
LEAD WIDTH		b1	0.17	0.2	0.23
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
	X	D	9 BSC		
	Y	E	9 BSC		
BODY SIZE	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.5 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
EP SIZE	X	M	3.9	4	4.1
	Y	N	3.9	4	4.1
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.08		
MOLD FLATNESS		eee	0.05		



SECTION G–G
SCALE: 100/1

NOTES
1. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
2. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLDPROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
4. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAM BAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.

5 EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8 Ordering Information

Part Number	Package	Shipping
iND83080	TQFP-48	2000pcs/Tape&Reel

9 Disclaimer

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